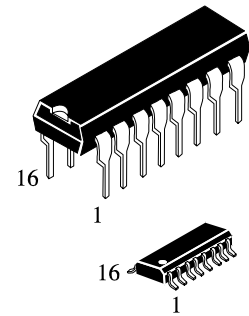


IW4043B

QUAD 3-STATE R/S LATCHES High-Voltage Silicon-Gate CMOS

The IW4043B types are quad cross-coupled 3-state CMOS NOR latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
1.0 V min @ 5.0 V supply
2.0 V min @ 10.0 V supply
2.5 V min @ 15.0 V supply



N SUFFIX
PLASTIC

D SUFFIX
SOIC

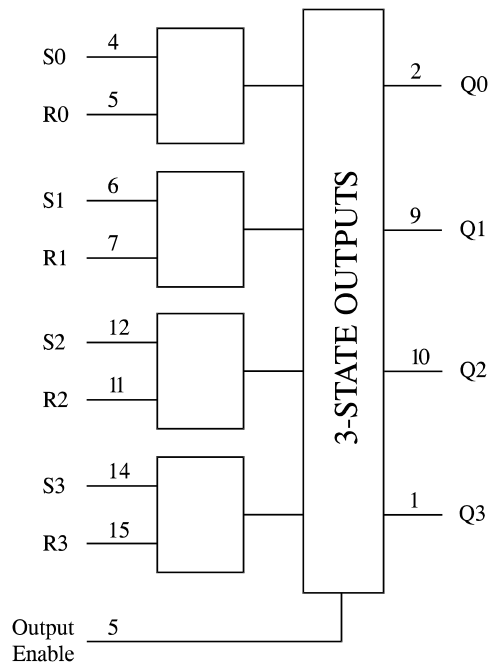
ORDERING INFORMATION

IW4043BN Plastic

IW4043BD SOIC

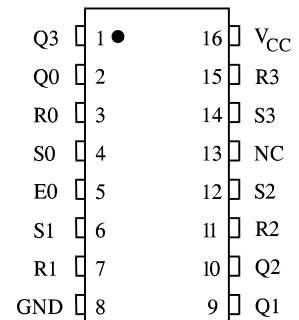
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 13 = NO CONNECTION
PIN 16 = V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs
S	R	OE	Q
X	X	L	High Impedance
L	L	H	No change
L	H	H	L
H	L	H	H
H	H	H	H

X = don't care

IW4043B

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

IW4043B

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.5 V or V _{CC} - 0.5V V _{OUT} = 1.0 V or V _{CC} - 1.0 V V _{OUT} = 1.5 V or V _{CC} - 1.5V	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} = 0.5 V or V _{CC} - 0.5V V _{OUT} = 1.0 V or V _{CC} - 1.0 V V _{OUT} = 1.5 V or V _{CC} - 1.5V	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{OZ}	Maximum Three State Leakage Current	Output in High-Impedance State V _{IN} = GND or V _{CC} V _{OUT} = GND or V _{CC}	18	±0.4	±0.4	±12.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	1	1	30	μA
			10	2	2	60	
			15	4	4	120	
			20	20	20	600	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

IW4043B

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			≥ -55 $^{\circ}\text{C}$	25°C	≤ 125 $^{\circ}\text{C}$	
t_{PHL} , t_{PLH}	Maximum Propagation Delay, SET or RESET to Q (Figure 1)	5.0	300	300	600	ns
		10	140	140	280	
		15	100	100	200	
t_{PHZ} , t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2,4)	5.0	230	230	460	ns
		10	110	110	220	
		15	80	80	160	
t_{PLZ} , t_{PZL}	Maximum Propagation Delay, Output Enable to Q (Figures 2,4)	5.0	180	180	360	ns
		10	100	100	200	
		15	70	70	140	
t_{THL} , t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS ($C_L=50\text{pF}$, $R_L=200\text{ k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			≥ -55 $^{\circ}\text{C}$	25°C	≤ 125 $^{\circ}\text{C}$	
t_w	Minimum Pulse Width, SET or RESET (Figure 3)	5.0	160	160	320	ns
		10	80	80	160	
		15	40	40	80	

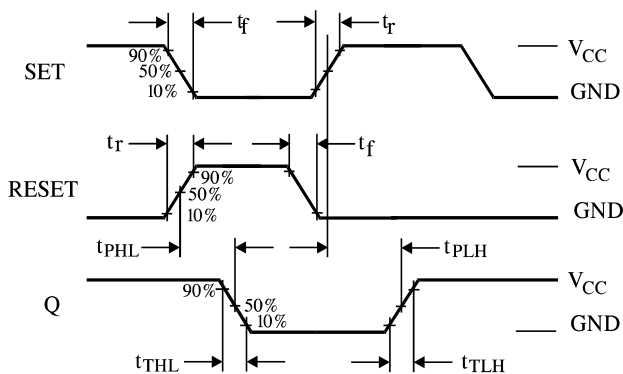


Figure 1. Switching Waveforms

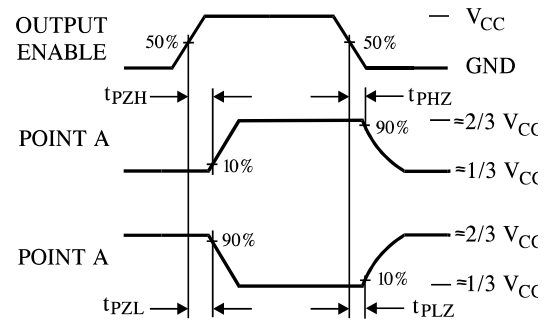


Figure 2. Switching Waveforms

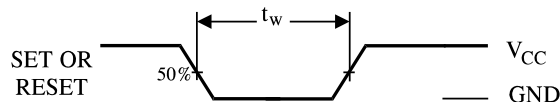
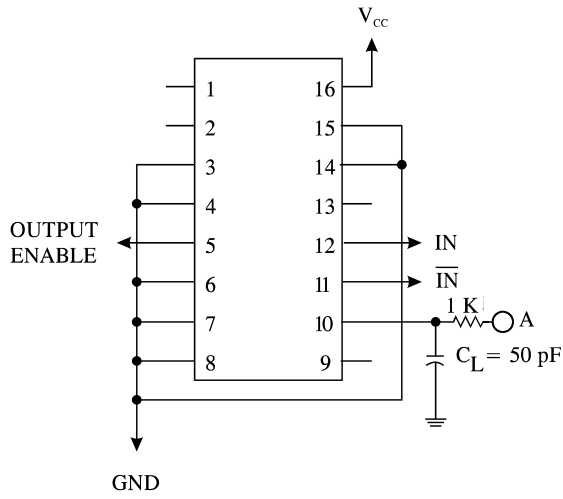


Figure 3. Switching Waveforms

IW4043B



TEST	IN	IN̄	A
t _{PHZ}	V _{CC}	GND	GND
t _{PLZ}	GND	V _{CC}	V _{CC}
t _{PZH}	V _{CC}	GND	GND
t _{PZL}	GND	V _{CC}	V _{CC}

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM (1/4 of the Device)

