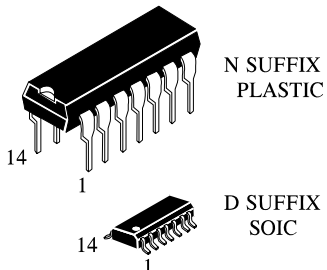


IN74HCT27A

Triple 3-Input NOR Gate

The IN74HCT27A is high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The device provide the Triple 3-input NOR function.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices

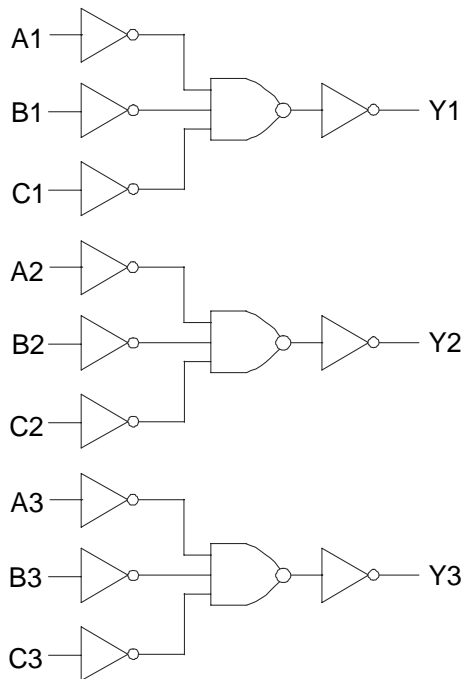


ORDERING INFORMATION

IN74HCT27AN	Plastic
IN74HCT27AD	SOIC
IZ74HCT27A	Chip

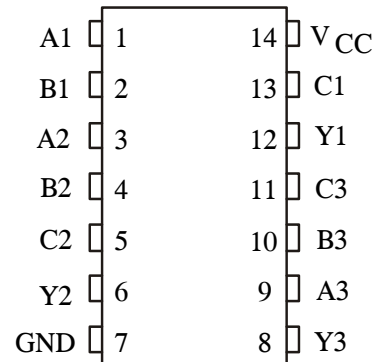
$T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
A	B	C	$Y = \overline{A + B + C}$
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			
	V _{CC} = 2.0 V	0	1000	ns
	V _{CC} = 4.5 V	0	500	
	V _{CC} = 6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} ≤ 0.1V or V _{OUT} ≥ V _{CC} - 0.1V I _{OUT} ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} ≤ 0.1V or V _{OUT} ≥ V _{CC} - 0.1V I _{OUT} ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ -20 μA	4.5	4.4	4.4	4.4	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ -4.0 mA	4.5	3.98	3.84	3.70	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	4.5	0.1	0.1	0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I _{IL}	Maximum Low-Level Input Leakage Current	V _{IN} = 0 V	5.5	-0.1	-1.0	-1.0	μA
I _{IH}	Maximum High-Level Input Leakage Current	V _{IN} = V _{CC}	5.5	0.1	1.0	1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = V _{CC} or 0 V I _{OUT} = 0 μA	5.5	2.0	20	40	μA
I _{CCT}	Maximum Additional Quiescent Supply Current on input pin	V _{IN} = 2.4V any one input, V _{IN} = 0 V or V _{CC} , others inputs I _{OUT} = 0 μA	4.5	≤ -55°C	25°C ÷ -125°C		mA
				2.9	2.4		

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t _{PHL} , t _{PLH}	Maximum Propagation Delay (Figure 1)	4.5	24	31	37	ns
t _{THL} , t _{TLH}	Maximum Output Transition Time (Figure 1)	4.5	15	19	22	ns
C _{IN}	Maximum Input Capacitance	5.0	10	10	10	pF

C _{PD}	Power Dissipation Capacitance (Per Gate)	T _A =25°C, V _{CC} =5.0 V			pF
	Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	54			

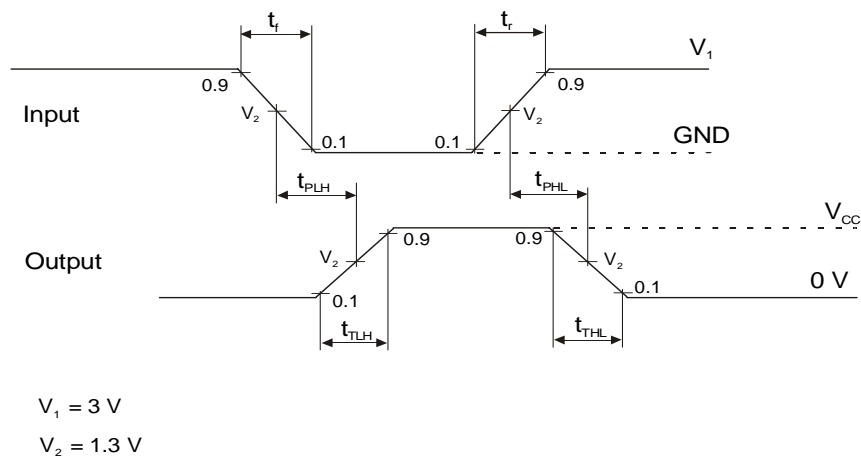


Figure 1. Switching Waveforms

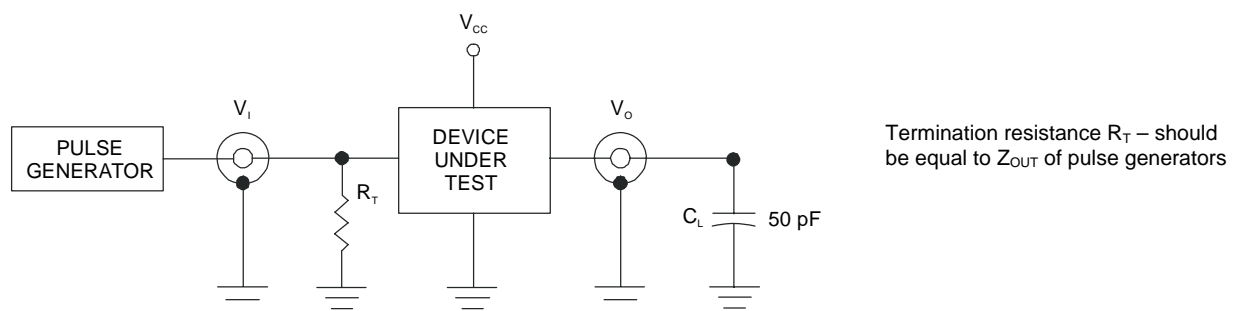
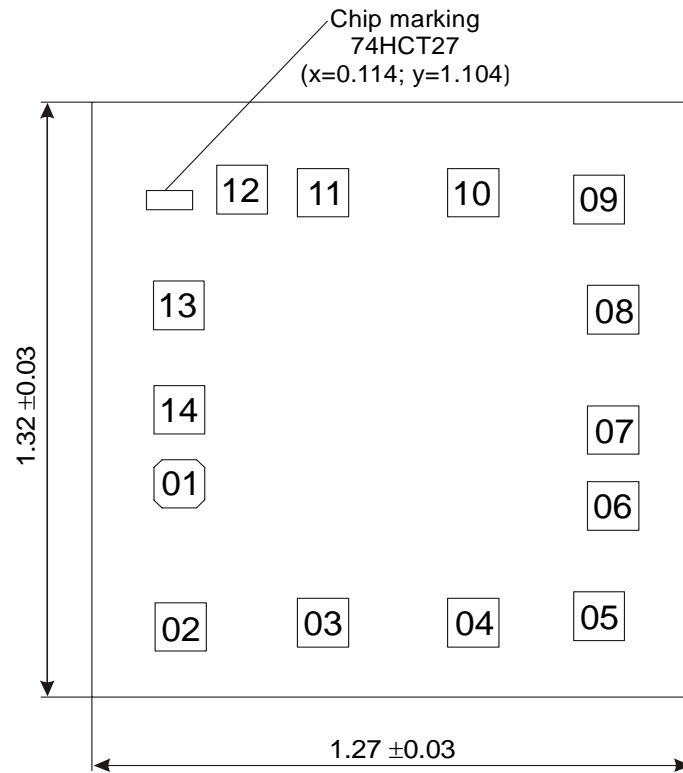


Figure 2. Test Circuit

CHIP PAD DIAGRAM IZ74HCT27A



Pad size 0.108 x 0.108 mm (Pad size is given as per passivation layer)
Thickness of chip 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	A1	0.129	0.442
02	B1	0.132	0.124
03	A2	0.433	0.133
04	B2	0.751	0.133
05	C2	1.017	0.148
06	$\bar{Y}2$	1.047	0.392
07	GND	1.047	0.561
08	A3	1.047	0.828
09	B3	1.017	1.073
10	C3	0.751	1.088
11	$\bar{Y}1$	0.433	1.088
12	H	0.262	1.095
13	C1	0.128	0.838
14	Vcc	0.129	0.606