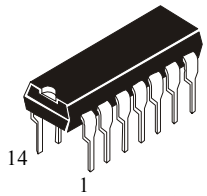
IN74HC32A

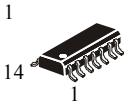
Quad 2-Input OR Gate
High-Performance Silicon-Gate CMOS

The IN74HC32A is identical in pinout to the LS/ALS32. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices



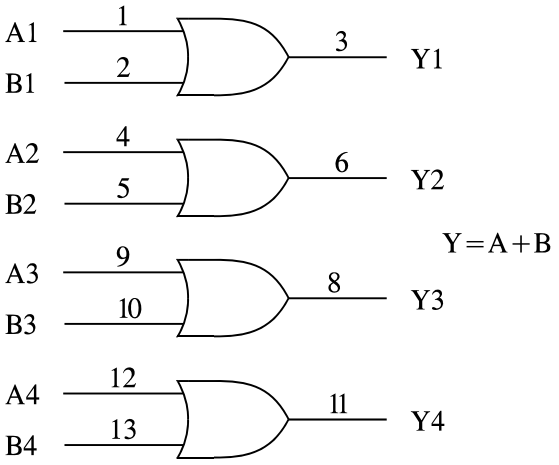
N SUFFIX
PLASTIC DIP



D SUFFIX
SOIC

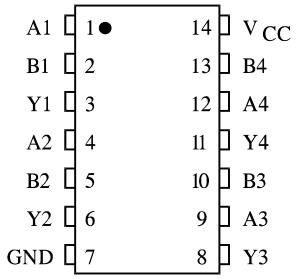
ORDERING INFORMATION
IN74HC32AN Plastic DIP
IN74HC32AD SOIC
IZ74HC32A chip
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 14 =V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

L – LOW voltage level

H – HIGH voltage level

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				-55°C to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}= V_{CC}-0.1 V $\|I_{OUT}\| \leq 20$ μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \leq 20$ μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA $\|I_{OUT}\| \leq 5.2$ mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= V_{IL} $\|I_{OUT}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}= V_{IL} $\|I_{OUT}\| \leq 4.0$ mA $\|I_{OUT}\| \leq 5.2$ mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0μA	6.0	1.0	10	40	μA

AC ELECTRICAL CHARACTERISTICS(C_L=50 pF,Input t_r=t_f=6.0 ns, V_{IH}=V_{CC}, V_{IL}=0 V)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			-55°C to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 20	pF

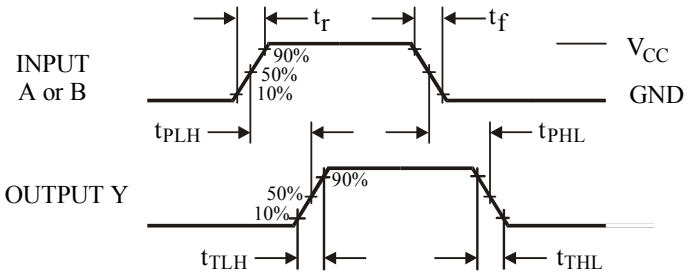
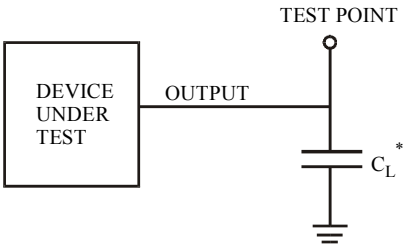


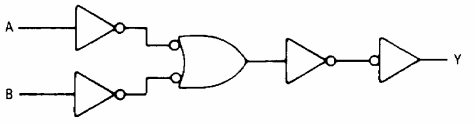
Figure 1. Switching Waveforms



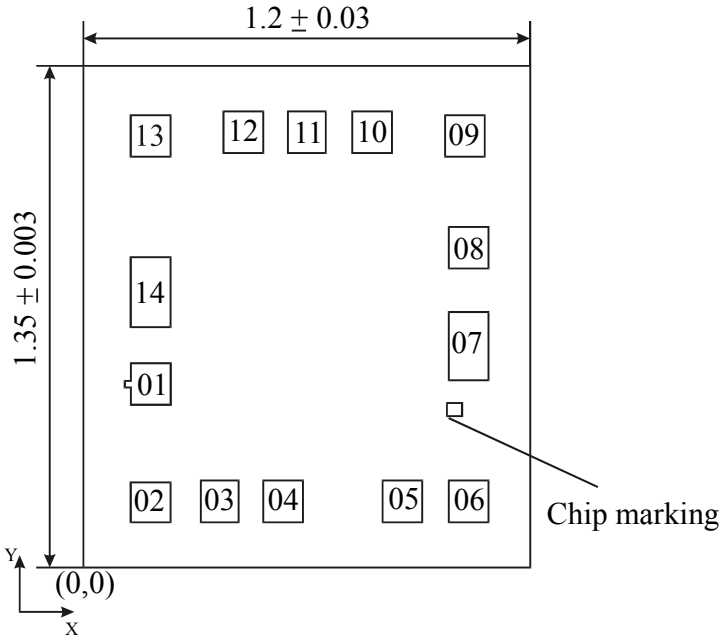
* Includes all probe and jig capacitance

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM
(1/4 of the Device)



CHIP PAD DIAGRAM



Chip marking :15-32
Location of marking (mm): left lower corner x = 0.978, y = 0.411; right lower corner x = 1.02, y = 0.447
Chip thickness: 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	A1	0.132	0.443	0.106×0.106
02	B1	0.132	0.126	0.106×0.106
03	Y1	0.315	0.129	0.106×0.106
04	A2	0.485	0.129	0.106×0.106
05	B2	0.802	0.129	0.106×0.106
06	Y2	0.981	0.129	0.106×0.106
07	GND	0.981	0.504	0.106×0.186
08	Y3	0.981	0.807	0.106×0.106
09	A3	0.971	1.105	0.106×0.106
10	B3	0.722	1.115	0.106×0.106
11	Y4	0.551	1.115	0.106×0.106
12	A4	0.381	1.115	0.106×0.106
13	B4	0.132	1.105	0.106×0.106
14	Vcc	0.132	0.650	0.106×0.186

Note: Location is given as per passivation layer