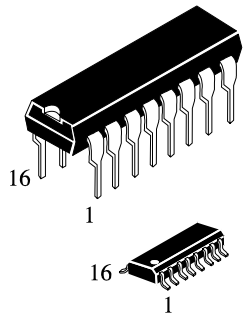
CMOS BCD-TO-7-SEGMENT
Latch Decoder Drivers

ICs IW4511B is using in high-performance computing systems with low power consumption in portable measuring equipments, communication devices with power supply from telephone networks, instruments using alternative power supplies (solar batteries, thermal elements) etc.

- Standard symmetrical output characteristic
- Operating Voltage Range: 3.0 to 18 V
- 100% testing for quiescent current at 20V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):

1.0 V min @ 5.0 V supply
2.0 V min @ 10.0 V supply
2.5 V min @ 15.0 V supply



N SUFFIX
PLASTIC

D SUFFIX
SOIC

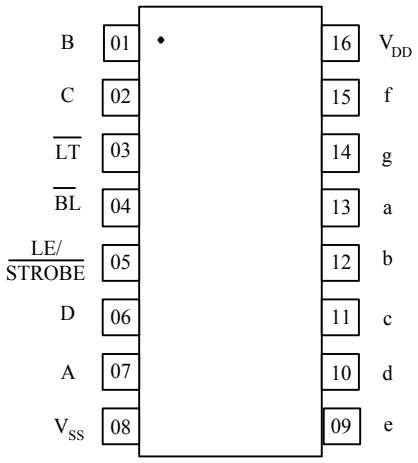
ORDERING INFORMATION

IW4503BN Plastic
IW4503BD SOIC
T_A = -55° to 125° C for all packages

PIN DESCRIPTION

Pin number	Symbol	Description
01	B	Input
02	C	Input
03	LT	Input
04	BL	Input
05	LE/STROBE	Input
06	D	Input
07	A	Input
08	V_{SS}	Common output
09	e	Output
10	d	Output
11	c	Output
12	b	Output
13	a	Output
14	g	Output
15	f	Output
16	V_{DD}	Supply

PIN ASSIGNMENT



INTEGRAL

TRUTH TABLE

Inputs							Outputs							Display
LE	BL	LT	D	C	B	A	a	b	c	d	e	f	g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X	*							*

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* - Depends on BCD code previously, applied when LE=L
X – Don't Care

MAXIMUM RATINGS

Symbol	Parameter	Recommended operating conditions		Maximum ratings		Unit
		min	max	min	max	
V_{DD}	DC Supply Voltage	3	18	-0.5	20	V
V_I	Input Voltage Range	-	-	-0.5	V_{DD}+0.5	V
V_O	Output Voltage Range	-	-	-0.5	V_{DD}+0.5	V
I_I	DC Input Current	-	-	-	±10	mA
P_D	Power dissipation per package	-	-	-	500*	mW
P_{tot}	Power Dissipation per Output Transistor	-	-	-	100	mW

*P_D for IW4511BN for temperature range - 55 - +100 °C and for ICs IW4511BD for temperature range - 55 - +65 °C

P_D for IW4511BN derate linearity at 12 mW/°C for temperature range +100 - +125°C.

P_D for IW4511BD derate linearity at 7 mW/°C for temperature range +65- +125°C.

STATIC ELECTRICAL CHARACTERISTIC

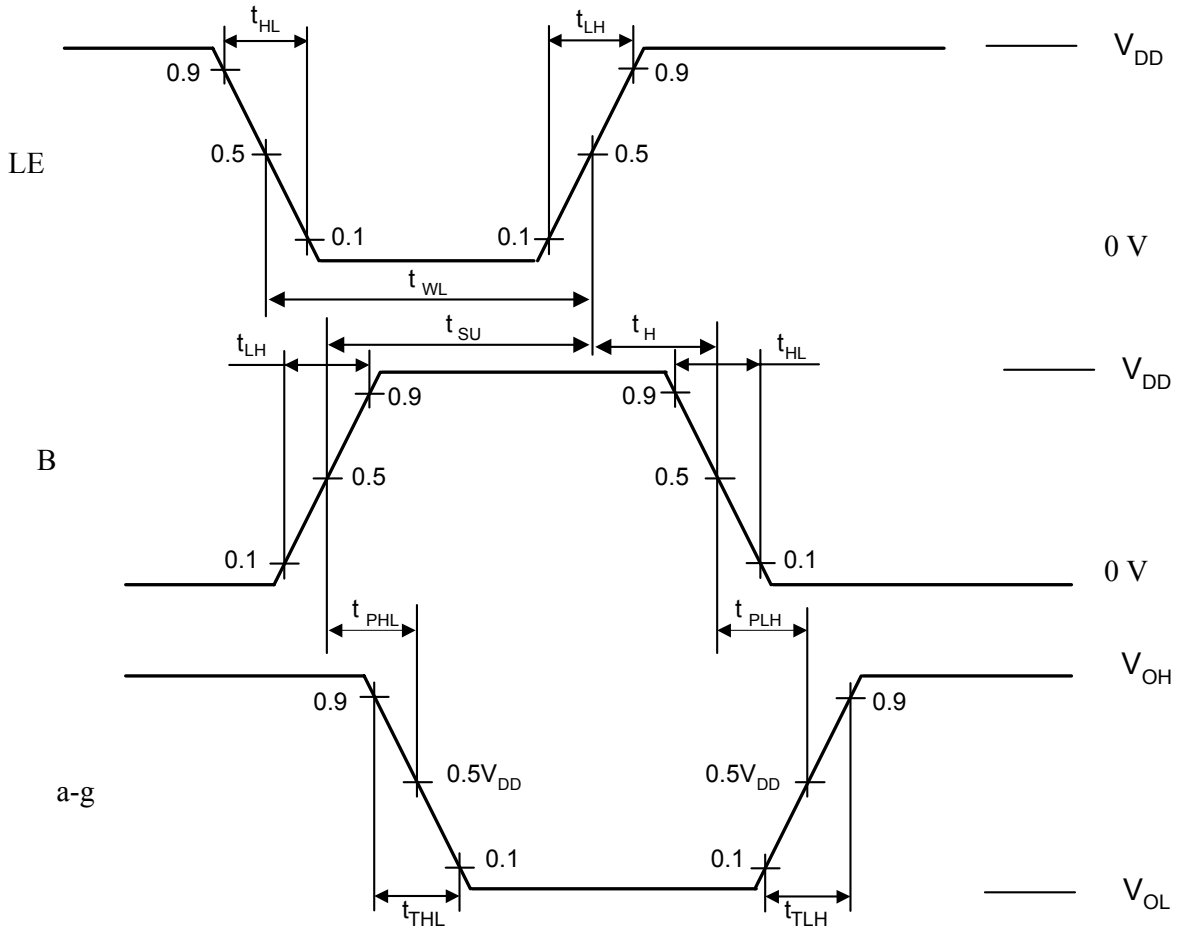
Sym-bol	Parameter	Test conditions	V_{DD}, V	Guaranteed Limits						Units
				-55°C		25°C		125°C		
				min	max	min	max	min	max	
V_{IH}	Minimum High-Level Input Voltage	V_O = 0.5 V or V_{DD}-1.2V	5.0	3.5	-	3.5	-	3.5	-	V
		V_O = 1.0 V or V_{DD}-1.2V	10	7.0	-	7.0	-	7.0	-	
		V_O = 1.5 V or V_{DD}-1.2V	15	11	-	11	-	11	-	
V_{IL}	Maximum Low -Level Input Voltage	V_O = 0.5 V or V_{DD}-1.2V	5.0	-	1.5	-	1.5	-	1.5	V
		V_O = 1.0 V or V_{DD}-1.2V	10	-	3.0	-	3.0	-	3.0	
		V_O = 1.5 V or V_{DD}-1.2V	15	-	4.0	-	4.0	-	4.0	
V_{OH}	High-Level Output Voltage	V_I = V_{SS} or V_{DD}	5.0	4.0	-	4.1	-	4.2	-	V
			10	9.0	-	9.1	-	9.2	-	
			15	14.0	-	14.1	-	14.2	-	
V_{OL}	Low-Level Output Voltage	V_I = V_{SS} or V_{DD}	5.0	-	0.05	-	0.05	-	0.05	V
			10	-	0.05	-	0.05	-	0.05	
			15	-	0.05	-	0.05	-	0.05	
I_{IL}	Low -Level Input Current	V_I = V_{SS}	18	-	-0.1	-	-0.1	-	-1.0	μA
I_{IH}	High -Level Input Current	V_I = V_{DD}	18	-	0.1	-	0.1	-	1.0	μA
I_{DD}	Quiescent Devices Current	V_I = V_{SS} or V_{DD}	5.0	-	5.0	-	5.0	-	150	μA
			10	-	10	-	10	-	300	
			15	-	20	-	20	-	600	
			20	-	100	-	100	-	3000	
I_{OL}	Output Low (Sink) Current	V_I = V_{SS} or V_{DD}								mA
		V_{OL} = 0.4 V	5.0	0.64	-	0.51	-	0.36	-	
		V_{OL} = 0.5 V	10	1.6	-	1.3	-	0.9	-	
		V_{OL} = 1.5 V	15	4.2	-	3.4	-	2.4	-	
I_{OH}	Output High (Source) Current	V_I = V_{SS} or V_{DD}								mA
		V_{OH} = 2.5 V	5.0	-1.6	-	-1.3	-	-0.9	-	
		V_{OH} = 4.6 V	5.0	-0.46	-	-0.37	-	-0.26	-	
		V_{OH} = 9.5 V	10	-0.98	-	-0.8	-	-0.55	-	
		V_{OH} = 13.5 V	15	-3.33	-	-2.7	-	-1.9	-	

DYNAMIC ELECTRICAL CHARACTERISTICS (C_L=50 pF, R_L = 200 kOhm, $t_{LH} = t_{HL} \leq 20$ ns)

Sym-bol	Parameter	Test conditions	V_{DD}, V	Guaranteed Limits						Unit
				-55 °C		25 °C		125 °C		
				min	max	min	max	min	max	
t_{PHL}	Propagation Delay Time High-to-Low Level Input (A-D)	Time diagram on the figure	5.0	-	1040	-	1040	-	2080	nc
			10	-	420	-	420	-	840	
			15	-	300	-	300	-	600	
	Propagation Delay Time High-to-Low Level Input BL	Time diagram on the figure	5.0	-	700	-	700	-	1400	
			10	-	350	-	350	-	700	
			15	-	250	-	250	-	500	
	Propagation Delay Time High-to-Low Level Input LT	Time diagram on the figure	5.0	-	500	-	500	-	1000	
			10	-	250	-	250	-	500	
			15	-	170	-	170	-	340	
t_{PLH}	Propagation Delay Time Low-to-High Level Input (A-D)	Time diagram on the figure	5.0	-	1320	-	1320	-	2640	nc
			10	-	520	-	520	-	1040	
			15	-	360	-	360	-	720	
	Propagation Delay Time Low-to-High Level Input BL	Time diagram on the figure	5.0	-	800	-	800	-	1600	
			10	-	350	-	350	-	700	
			15	-	300	-	300	-	600	
	Propagation Delay Time Low-to-High Level Input LT	Time diagram on the figure	5.0	-	300	-	300	-	600	
			10	-	150	-	150	-	300	
			15	-	100	-	100	-	200	
t_{THL}	Transition Time High-to-Low Level	Time diagram on the figure	5.0	-	310	-	310	-	620	nc
			10	-	185	-	185	-	370	
			15	-	160	-	160	-	320	
t_{TLH}	Transition Time Low-to-High Level	Time diagram on the figure	5.0	-	80	-	80	-	160	nc
			10	-	60	-	60	-	120	
			15	-	50	-	50	-	100	
t_{SU}	Set-Up Time (A-D) as per LE	Time diagram on the figure	5.0	150	-	150	-	300	-	nc
			10	70	-	70	-	140	-	
			15	40	-	40	-	80	-	
t_H	Hold Time (A - D) after LE	Time diagram on the figure	5.0	0	-	0	-	0	-	nc
			10	0	-	0	-	0	-	
			15	0	-	0	-	0	-	
t_{WL}	LE Pulse Width	Time diagram on the figure	5.0	400	-	400	-	800	-	nc
			10	160	-	160	-	320	-	
			15	100	-	100	-	200	-	

CAPACITANCE

Symbol	Parameter	V_{DD}, v	Guaranteed Limits		Unit
			min	max	
C_{IN}	Input Capacitance	-	-	7.5	pF



Time diagram when taking dynamic parameters