POWER FACTOR CORRECTOR CIRCUIT

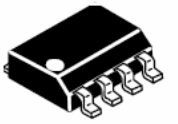
functional equivalent L6562 STMicroelectronics

DESCRIPTION

The power factor correction is specifically designed for use as a preconverter in electronic ballast and in autonomous power converter applications. The circuit is purposed for AC-DC adapters, battery chargers and some other applications.

The circuit performs voltage-current phase shift compensation by means of creation of phase lead in some nodes of circuit to reduce active parasitic losses in the conductors and distributive equipment.

The IC is available in SO-8 plastic (MS-012AA) case



Plastic case
MS-012AA (SO-8)

Fig. 1 – Device view

Features:

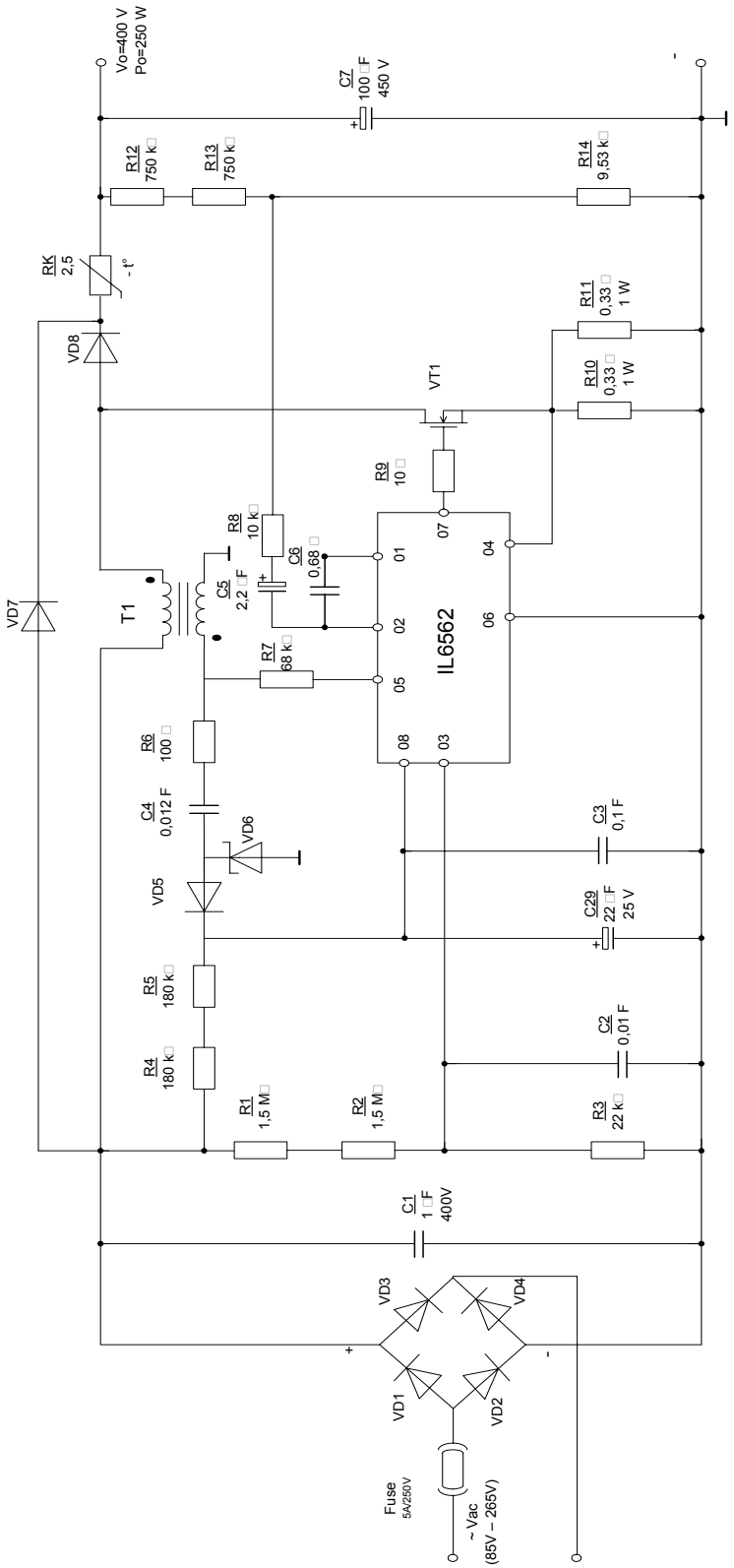
- Transition-mode control of PFC
- Original multiplier design minimizes THD of AC input current
- Precise adjustable output overvoltage protection
- Low start-up supply current
- Low (≤70μa) stand-by supply current
- Operating supply current not exceed 5mA
- Extended supply voltage range up to 22V
- Build-in filter on current sense
- Disable function
- Precise internal reference voltage source
- Two gate output stage r with undervoltage pull-down and voltage regulator

SO-8 (MS-012AA.) case

The weight of IC not exceeds 0,15 g.

Table 1 – Pin description

Pin number	Symbol	Function
01	INV	Inverting input of the error amplifier.
02	COMP	Output of the error amplifier.
03	MULT	Main input to the multiplier.
04	CS	Input to the PWM comparator.
05	ZCD	Control input
06	GND	Ground.
07	GD	Gate driver output.
08	V_{cc}	Supply voltage pin



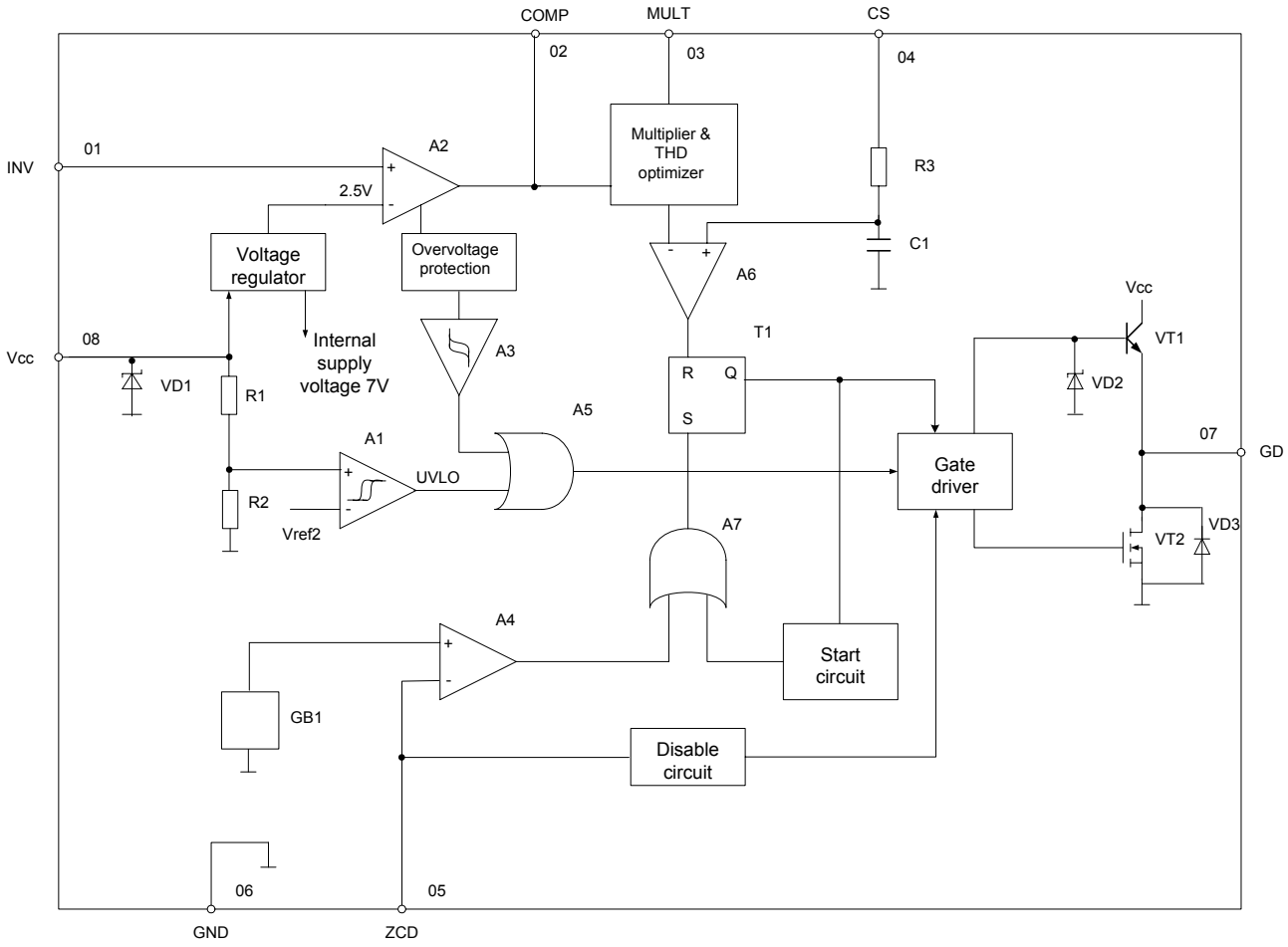
T1 – transformer

VD1 – VD5, VD7, VD8 – diodes;

VD6 – Shottky diode

VT1 – transistor;

Fig. 2 –Typical application diagram



A1, A6 – comparators
A2 – error amplifier
A3 – Schmitt trigger
A4 – zero current detector
A5, A7 – «AND» gates
A8 – trigger
C1 – capacitor 5 pF
G1- reference voltage source 1,6 … 2,1 V
R1, R2, R3 – resistors
VD1, VD2 – zeners
VD3 – protection diode
VT1, VT2 – transistors

Fig. 3 – Block diagram

Table 2 – Recommended operation mode

Symbol	Parameter	Target		Unit
		Min.	Max.	
U_{CC}	Supply voltage	-	22,5	V
U_{1-4}	Analog inputs & outputs voltage (pins 1-4)	- 0,3	8	V
$I_{ZCDsink}$	Zero current detector max. current (sink)		10	mA
$I_{ZCDsource}$	Zero current detector max. current (sourse)		- 50	mA
P_{tot}	Power dissipation (at T_A = 50 °C)		0,65	W
T_A	Ambient temperature	- 60[1)]		°C
T_J	Operating junction temperature	- 60[1)]	150	°C
T_{stg}	Storage temperature	- 60	150	°C
[1)] Ambient temperature is indicated				

Table 3 – Maximum rating

Symbol	Parameter	Target		Unit
		Min.	Max.	
U_{CC}	Supply voltage	10,3	22	V
T_A	Ambient temperature	- 25	-	°C
T_J	Operating junction temperature	- 25[1)]	125	°C
[1)] Ambient temperature is indicated				

Table 4 – Electric parameters -25[1)] ≤T_J ≤125 °C, U_{CC} = 12 V, C_L = 1 nF

Symbol	Parameter	Measurement mode	Target		Unit
			Min.	Max.	
Supply voltage					
U_{CC}	Supply voltage range	After turn-on	10,3	22,0	V
U_{CCon}	Turn-on threshold voltage	-	11,0	13,0	V
U_{CCOff}	Turn-off threshold voltage	-	8,7	10,3	V
U_{HYS}	Hysteresis	-	2,2	2,8	V
U_Z	Zener voltage	I_{CC} = 20 mA	22	28	V
Supply current					
$I_{start-up}$	Start-up current	Before turn-on, U_{CC} = 11 V		70	µA
I_q	Quiescent current	After turn-on		3,75	mA
I_{CC}	Operating supply current	70 kHz		5,0	mA
I_q	Quiescent current	During operation overvoltage protection (either static or dynamic) or U_{ZCD} = 150 mV		2,2	mA
Multiplier input					
I_{MULT}	Input bias current	U_{VFF} = 0 ÷ 4 V		-1,0[2)]	µA
$\Delta U_{CS}/\Delta U_{MULT}$	Output signal max. slope	U_{MULT} = 0 ÷ 0.5V U_{COMP} = Upper clamp (High level regulation)	1,65		V/V
K	Multiplier gain [2)]	U_{MULT} = 1 V, U_{COMP} = 4 V	0,5	0,7	1/V

Table 4 continued

Symbol	Parameter	Measurement mode	Value		Unit
			Min.	Max.	
Error amplifier					
U_{INV}	Voltage feedback input threshold	T_j = 25 °C	2,465	2,535	V
		10,3 V < U_{cc} < 22 V	2,44	2,56	V
U_{REG}	Line regulation	U_{cc} = 10,3 V ÷ 22 V		5,0	mV
I_{INV}	Input bias current	U_{INV} = 0 ÷ 3 V		- 1,0	µA
Gv	Voltage gain	Open loop	60,0	-	dB
$I_{O\ COMP}$	Source current	U_{COMP} = 4 V, U_{INV} = 2,4 V	- 2,0	- 5,0	mA
$I_{I\ COMP}$	Sink Current	U_{COMP} = 4 V, U_{INV} = 2,6 V	2,5	-	mA
$U_{H\ COMP}$	High level clamp voltage	I_{SOURCE} = 0,5 mA	5,3	6,7	V
$U_{L\ COMP}$	Low level clamp voltage	I_{SINK} = 0,5 mA	2,1	2,4	V
Current sense comparator					
I_{CS}	Input Bias Current	U_{CS} = 0	-	- 1,0 [2)]	µA
$t_{d(H-L)}$	Propagation delay	-	-	350	ns
$U_{CS\ clamp}$	Current sense reference voltage	U_{COMP} = Upper clamp (High level regulation)	1,6	1,8	V
Zero current detector					
U_{ZCDH}	High level clamp voltage	$I_{ZCD\ H}$ = 2,5 mA	5,0	6,5	V
U_{ZCDL}	Low level clamp voltage	$I_{ZCD\ L}$ = - 2,5 mA	0,3	1,0	V
I_{ZCDsrc}	Source current	[3)]	- 2,5	- 5,5	mA
I_{ZCDsnk}	Sink current	-	2,5	-	mA
U_{ZCDdis}	Disable (turn-off) threshold	-	150	250	mV
U_{ZCDen}	Restart threshold	-	-	350	mV

Table 4 Continued

Symbol	Parameter	Measurement mode	Value		Unit
			Min.	Max.	
I_{ZCDres}	Restart current after disable	-	30,0	-	μA
Start-up circuit					
t_{START}	Start period	-	75,0	300	μs
Overvoltage protection					
I_{OVP}	Dynamic overvoltage protection turn-on current	-	35,0	45,0	μA
$U_{GYS\ (OVP)}$	Static overvoltage protection hysteresis current	-	2,1	2,4	V
Gate driver					
U_{OH}	Dropout voltage	$I_{GD\ SOURCE}$ = 20 mA [3]	-	2,6	V
U_{OL}		$I_{GD\ SOURCE}$ = 200 mA [3]	-	3,0	V
		$I_{GD\ SINK}$=200mA [4]	-	1,9	V
t_f	Output signal fall time	-	-	70,0	ns
t_r	Output signal rise time	-	-	80,0	ns
V_{Oclamp}	Output clamp voltage	$I_{GD\ SOURCE}$ = 5 mA; U_{cc} = 20 V	10,0	15,0	V
-	UVLO (under voltage lock-out) saturation	U_{CC} = 0 ÷ UC_{Con}, I_{SINK} = 10 mA	-	1,1	V

Notes:

1.Symbol description:

- OVP – overvoltage protection;
- U_{ZCD} – pin 05 voltage;
- U_{MULT} – pin 03 voltage;
- U_{COMP} –pin 02 voltage;
- Upper clamp – high level of voltage stabilization;
- $I_{GD\ SOURCE}$ –current outflowing thought pin 07;
- $I_{GD\ SINK}$ – current inflowing thought pin 07.

2.Minus indicates current direction (source). Magnitude is considered as current value.

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[1] Ambient temperature is indicated

[2] Multiplier output voltage U_{CS}, V, is calculated by formula:

$$U_{cs} = K \times U_{MULT} \times (U_{COMP} - 2{,}5\ V), \quad (1)$$

K – multiplier gain ratio, 1/V;
U_{MULT} – linear voltage range, V;
U_{COMP} – pin 02 voltage, V

[3] $U_{OH} = U_{CC} - U_{GDH}$, $U_{OL} = U_{GDL}$, (2)
U_{GDH} and U_{GDL} are high level and low level GD pin voltages relative to GND pin.

Table 5 – Typical parameters

Symbol	Parameter	Measurement mode	Typical value	Unit
GB	Error amplifier gain-bandwidth product	-	1,0	MHz
$U_{CSoffset}$	Current sense comparator offset voltage	U_{MULT} = 0	30,0	mV
		U_{MULT} = 2,5 V	5,0	mV
U_{ZCDA}	Zero current detector voltage (positive-going edge)	-	2,1	V
U_{ZCDT}	Zero current detector voltage (negative-going edge)	-	1,6	V
I_{ZCDb}	Input bias current of zero current detector	U_{ZCD} = 1 ÷ 4,5 V	2,0	µA
I_{HYS}	Overvoltage protection hysteresis current	-	30,0	µA
U_{MULT}	Linear voltage range	-	0÷3,0	V
Note - Typical value is arithmetic mean of parameter value, of measured sampling.				

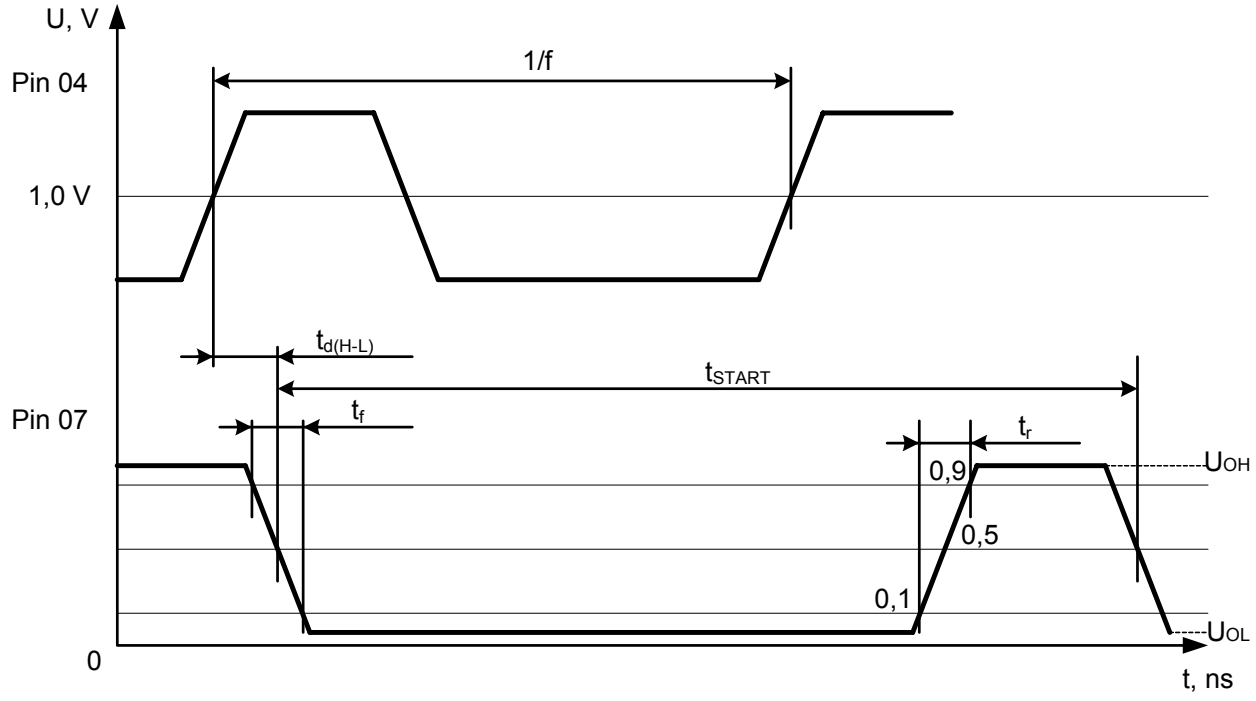


Fig. 4 – Output signal fall time t_f, output signal rise time t_r, propagation delay $t_{d(H-L)}$, timer restart time t_{START} timing diagram

Functional Description

IC consists of the following units:

- Multiplier;
- Voltage regulator;
- Over voltage protection;
- Zero-current detector;
- Control gate;
- Start circuit;
- Disable circuit.

IL6562D is a current-mode PFC (power factor correction) controller. IC operation is performed in transition mode (TM).

Power factor λ is a complex indicator of the power supply efficiency, and is defined as the ratio between active (useful) and total (active and reactive) power consumption of the voltage converter.

$$\lambda = \frac{P_{IN.ACT.}}{P_{IN.TOT.}}, \qquad (1)$$

$P_{IN.ACT.}$ – active power consumption voltage converter, W;

$P_{IN\ .\ TOT.}$ – total power consumption, W.

Power factor indicates how much of the consumption energy from primary network goes to the transformation, and how much energy does not make a useful work (reactive load), forcing the hardware designer to use wire with a larger cross-section to avoid overheating.

In practice, the absence of PFC leads to the following . In the traditional construction of the power supply when the input circuit contain rectifier bridge and smoothing capacitor (reactive load), the current is consumed from the supply line in a form of short pulses which coincide with the peak value of input voltage, in higher harmonics of current appear in the supply line form of voltage in the line is distorted. Principal danger are all multiples of third harmonic current. These harmonics of each phase are summed up in a zero wire of 3-phase line, which can lead to overheating and fire isolation. PFC task is to form a log-term supply current sinusoidal phase coincides with the input voltage, ie, make the power supply IC to the primary line of the active load.

IL6562D is a single stage PWM controller with integrated power factor correction. The IC allow to create both power supply sources: a galvanically decoupled and galvanically connected to the primary power supply line with the current stabilization. Output reactive power can vary from tens to hundreds of watts and even more (up to 250 watts). Maximum power depends on the parameters of an external transistor and overall capacity of the transformer.

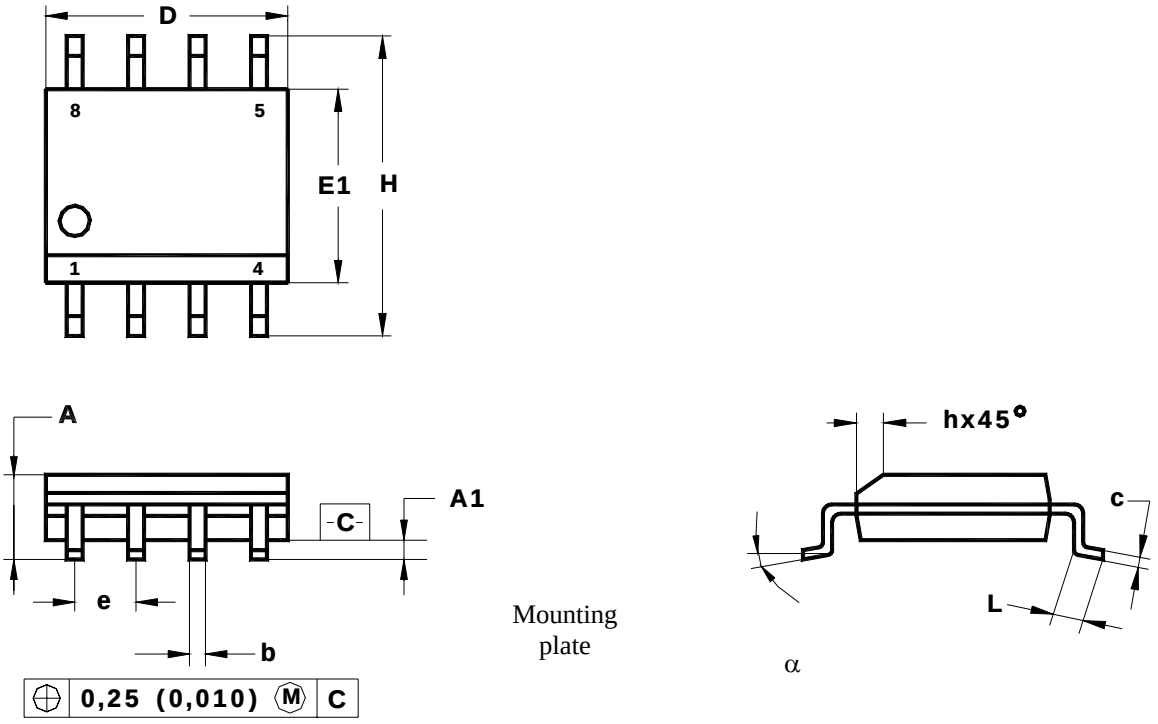
IL6562D designed to control the converters, operating in the a critical conduction mode where the PWM circuit is in self-oscillating mode enabling is provided by the detector zero-point energy of the transformer, and disabling by current-sense comparator. Zero-power detector allows you to disable the controller's output at a low load to avoid dangerous overvoltages.

The input voltage obtained after the input rectifier is fed thought the input resistor divider to MULT pin of the chip. The input voltage shape serves a reference signal for the PWM converter, and sets the current through the power switch, so consumption current of the converter current is sinusoidal and is at a proper phase with the supply voltage. So at the converter output the stable voltage is obtained. High-linear multiplier includes a special circuit that could reduce the distortion of input AC current, thus extending the range of operation with an extremely low total value of the nonlinear distortion even for a wide range of the load.

The output voltage is controlled by an error amplifier, and precise (1% at TA = 25 ° C) internal reference voltage.
The output stage of the gate driver with two stable states with a large source and sink current, can be applied to drive a power MOSFET or IGBT transistors, which together with other features makes the IC excellent low-cost solution for pulsed power supplies.
IL6562D is characterized by extremely low current consumption (less than 70 uA for standby mode and no more than 5 mA for operating mode) and includes a disable function.
Efficient two-stage overvoltage protection, including safe control surges which can occur either at startup or at break load.

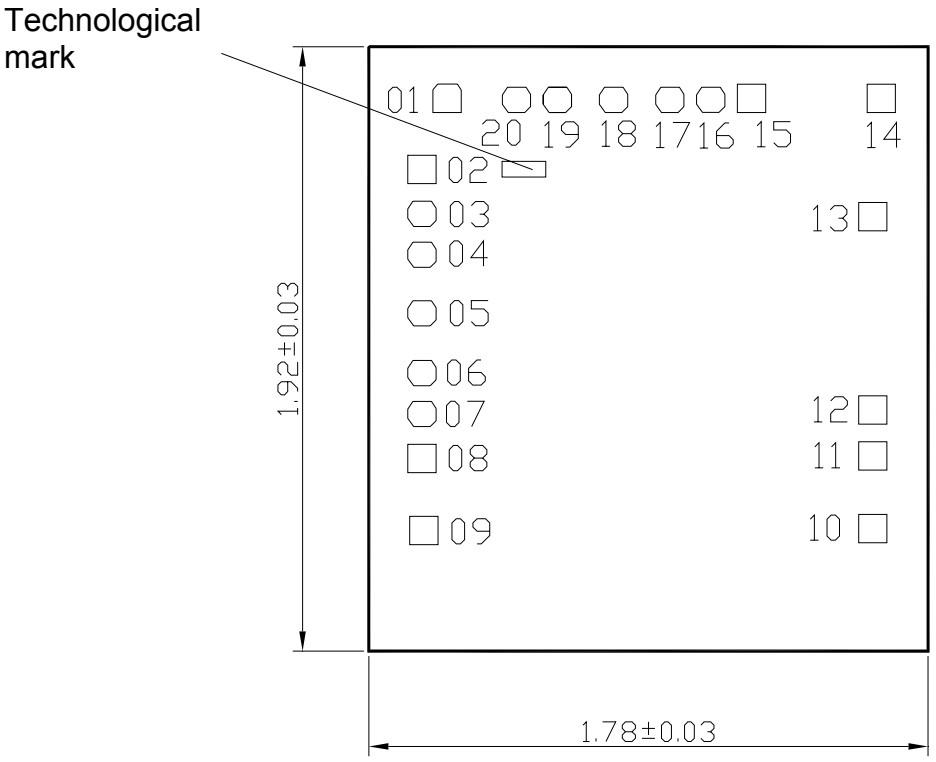
Pin purpose description
- INV (01) Inverting input of the error amplifier. The information on the output voltage of the PFC preregulator is fed into the pin through a resistor divider.
- COMP (02) Output of the error amplifier. A compensation network is placed between this pin and INV (pin 01) to achieve stability of the voltage control loop and ensure high power factor and low THD.
- MULT (03) - Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
- CS (04) - PWM comparator input. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off.
- ZCD (05) – Control pin This pin controls increasing of the inductor's demagnetization for transition-mode operation. A negative level turns-on MOSFET.
- GND (06) – Ground pin.(Common)
- GD (07) - Gate driver output. The output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is limited at about 12V to avoid excessive gate voltages in case the pin is supplied with Ucc >12V.
- Vcc (08) - Supply voltage pin . The supply voltage upper limit is extended to 22V to provide wider range for supply voltage changes.

D SUFFIX PLASTIK SOP
(MS-012AA)



	D	E1	H	b	e	α	A	A1	c	L	h
mm											
min	4.80	3.80	5.80	0.33		0°	1.35	0.10	0.19	0.41	0.25
max	5.00	4.00	6.20	0.51	1.27	8°	1.75	0.25	0.25	1.27	0.50
inches											
min	0.1890	0.1497	0.2284	0.013		0°	0.0532	0.0040	0.0075	0.016	0.0099
max	0.1968	0.1574	0.2440	0.020	0.100	8°	0.0688	0.0090	0.0098	0.050	0.0196

Fig. 3 –MS-012AA Package dimensions



Technological mark «6562» has coordinates, mm: left bottom corner x = 0,235 , y = 1,550.

Fig. 6– Chip outline drawing

Table 6 – Contact pad location table

Contact pad number	Coordinates (Left bottom corner), mm		Contact pad dimensions, mm
	X	Y	
01	0,204	1,711	0,090x0,090
02	0,124	1,485	0,090x0,090
03	0,124	1,349	0,090x0,080
04	0,124	1,219	0,090x0,080
05	0,124	1,033	0,090x0,080
06	0,124	0,843	0,090x0,080
07	0,124	0,713	0,090x0,080
08	0,124	0,567	0,090x0,090
09	0,130	0,338	0,090x0,090
10	1,559	0,344	0,090x0,090
11	1,559	0,575	0,090x0,090
12	1,559	0,721	0,090x0,090
13	1,559	1,335	0,090x0,090
14	1,586	1,711	0,090x0,090
15	1,173	1,711	0,090x0,090
16	1,043	1,711	0,090x0,080
17	0,913	1,711	0,090x0,080
18	0,734	1,711	0,090x0,080
19	0,555	1,711	0,090x0,080
20	0,425	1,711	0,090x0,080

Note- Coordinates and size of the contact pads are indicated by the layer «Passivation»