8-BIT SHIFT REGISTER

High-Voltage Silicon-Gate CMOS

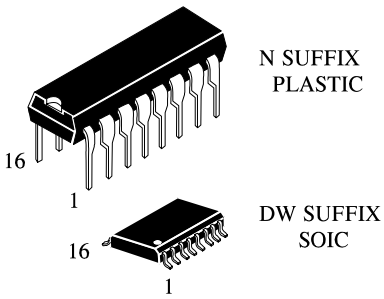
The IW4021B is an Edge-Triggered 8-Bit Shift Register (Parallel-to-Serial Converter) with a synchronous Serial Data Input (D_S), a Clock Input (CP), an asynchronous active HIGH Parallel Load Input (PL), eight asynchronous Parallel Data Inputs (P_0-P_7) and Buffered Parallel Outputs from the last three stages (Q_5-Q_7).

Information on the Parallel Data Inputs (P0-P7) is asynchronously loaded into the register while the Parallel Load Input (PL) is HIGH, independent of the Clock (CP) and Serial Data (D_S) inputs. Data present in the register is stored on the HIGH-to-LOW transition of the Parallel Load Input (PL).

When the Parallel Load Input is LOW, data on the Serial Data Input (D_S) is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):

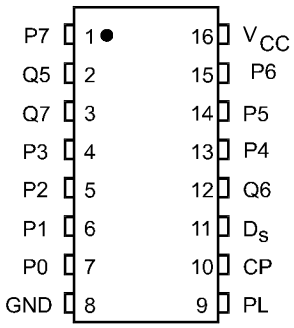
1.0 V min @ 5.0 V supply
2.0 V min @ 10.0 V supply
2.5 V min @ 15.0 V supply



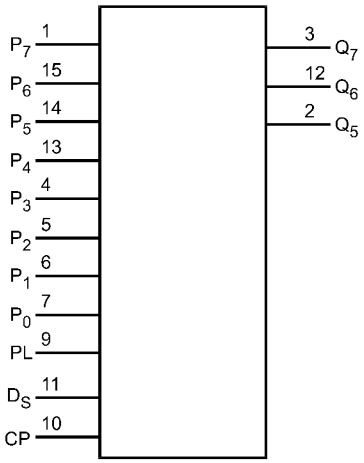
ORDERING INFORMATION

IW4021BN Plastic
IW4021BDW SOIC
T_A = -55° to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

FUNCTION TABLE

SERIAL OPERATION:

t	CP	D_S	PL	Q_5 t=n+6	Q_6 t=n+7	Q_7 t=n+8
n	⎍	0	0	0		
n+1	⎍	1	0	1	0	
n+2	⎍	0	0	0	1	0
n+3	⎍	1	0	1	0	1
	⎎	X	0	Q_5	Q_6	Q_7

PARALLEL OPERATION:

CP	D_S	PL	P_5	P_6	P_7	Q_5	Q_6	Q_7
X	X	1	D	D	D	D	D	D

X = don't care
D = 1 or 0

INTEGRAL

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V V_{OUT}=1.0 V or V_{CC} - 1.0 V V_{OUT}=1.5 V or V_{CC} - 1.5 V	5.0 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V V_{OUT}=1.0 V or V_{CC} - 1.0 V V_{OUT}=1.5 V or V_{CC} - 1.5 V	5.0 10 15	1.5 3 4	1.5 3 4	1.5 3 4	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0 10 15 20	5.0 10 20 100	5.0 10 20 100	150 300 600 3000	μA
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC} V_{OL}=0.4 V V_{OL}=0.5 V V_{OL}=1.5 V	 5.0 10 15	 0.64 1.6 4.2	 0.51 1.3 3.4	 0.36 0.9 2.4	mA
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC} V_{OH}=2.5 V V_{OH}=4.6 V V_{OH}=9.5 V V_{OH}=13.5 V	 5.0 5.0 10 15	 -2.0 -0.64 -1.6 -4.2	 -1.6 -0.51 -1.3 -3.4	 -1.15 -0.36 -0.9 -2.4	mA

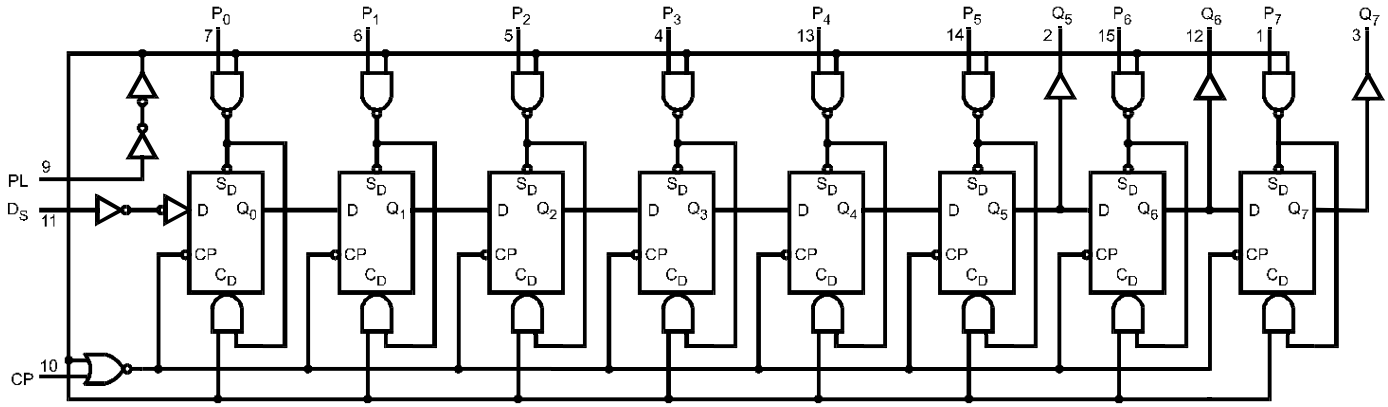
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			≥-55 °C	25°C	≤125 °C	
f_{max}	Maximum Clock Frequency	5.0 10 15	3.0 6.0 8.5	3.0 6.0 8.5	1.5 3.0 4.25	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Qn	5.0 10 15	320 160 120	320 160 120	640 320 240	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, PL to Qn	5.0 10 15	320 160 120	320 160 120	640 320 240	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C_{IN}	Maximum Input Capacitance	5.0		7.5		pF

TIMING REQUIREMENTS(C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			≥-55 °C	25°C	≤125 °C	
t_w	Minimum Pulse Width CP	5.0 10 15	160 80 50	160 80 50	320 160 100	ns
t_w	Minimum Pulse Width PL	5.0 10 15	180 80 50	180 80 50	360 160 100	ns
t_{su}	Minimum Setup Time, D_S toCP	5.0 10 15	120 80 60	120 80 60	240 160 120	ns
t_{su}	Minimum Setup Time, Pn to PL	5.0 10 15	50 30 20	50 30 20	100 60 40	ns
t_h	Minimum Hold Time, D_S toCP	5.0 10 15	0 0 0	0 0 0	0 0 0	ns
t_h	Minimum Hold Time, Pn to PL	5.0 10 15	0 0 0	0 0 0	0 0 0	ns
t_{rec}	Minimum Recovery Time PL	5.0 10 15	280 140 100	280 140 100	560 240 200	ns
t_r, t_f	Maximum Input Rise or Fall Time	5.0 10 15	15 15 15	15 15 15	15 15 15	μs

EXPANDED LOGIC DIAGRAM



INTEGRAL