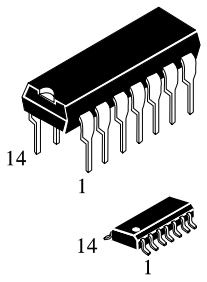
IW4066B

Quad Bilateral Switch
High-Voltage Silicon-Gate CMOS



ORDERING INFORMATION

IW4066BN	Plastic DIP
IW4066BD	SOIC
IZ4066B	chip

T_A = -55° to 125° C for all packages

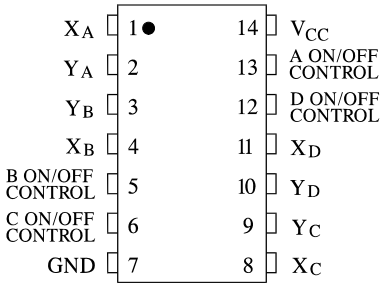
The IW4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. In addition, the on-state resistance is relatively constant over the full input-signal range.

The IW4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. (As show in Fig.1.) The well of the n-channel device on each switch is either tied to the input when the switch is on or to GND when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

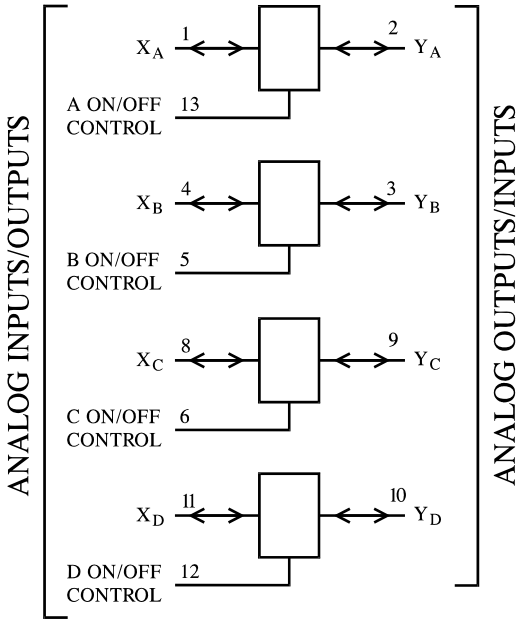
The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1.0 V min @ 5.0 V supply
  2.0 V min @ 10.0 V supply
  2.5 V min @ 15.0 V supply

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 14 =V_{CC}
PIN 7 = GND

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

H = high level
L = low level

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air	500*[1]	mW
P_{tot}	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SO Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*[1] - for Plastic DIP from -55° to +100°C, for SO Package from -55° to +65°C.
+Derating - Plastic DIP: - 12 mW/°C from 100° to 125°C
SO Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}	DC Input Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused digital pins must be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated.

DC ELECTRICAL CHARACTERISTICS Digital Section

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				≥ -55 °C	≤ 25 °C	≤ 125 °C	
V_{IHC}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs		5 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V_{ILC}	Maximum Low -Level Input Voltage, Channel-Select or Enable Inputs		5.0 10 15	1 2 2	1 2 2	1 2 2	V
I_{IN}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V_{IN}=V_{CC} or GND	18	±0.1	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)		5.0 10 15 20	0.25 0.5 1 5	0.25 0.5 1 5	7.5 15 30 150	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				≥ -55 °C	≤ 25 °C	≤ 125 °C	
R_{ON}	Maximum "ON" Resistance	V_C= V_{CC} V_{IS} = GND to V_{CC}	5.0 10 15	800 310 190	1000 400 240	1150 550 320	Ω
ΔR_{ON}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V_C= V_{CC} V_{IS} = GND to V_{CC}	5.0 10 15	- - -	15* 10* 5*	- - -	Ω
I_{OFF}	Maximum Off- Channel Leakage Current, Any One Channel	V_{IL} = 0 V, V_{IH} = 18 V	18	±0.1	±0.1	±1.0	μA
	Maximum Off- Channel Leakage Current, Common Channel	V_{IL} = 0 V, V_{IH} = 18 V	18	±0.1	±0.1	±1.0	

* - Typical Value

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f≤20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	25°C	≤125°C	Unit
t_{PHL}(t_{PLH})	Maximum Propagation Delay, Analog Input to Analog Output (Figure 2) R_L=200 kΩ	5.0 10 15	40 20 15	40 20 15	40 20 15	ns
t_{PLZ}(t_{PHZ}), t_{PZL}(t_{PZH})	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figure 3) R_L=1 kΩ	5.0 10 15	70 40 30	70 40 30	70 40 30	ns
C_{IN}	Maximum Input Capacitance	5	-	7.5	-	pF
$C_{I/O}$	Maximum Capacitance V_{CC} = GND= -5V					pF
	Analog Input	5	-	8*	-	
	Analog Output	5	-	6*	-	
	Between Analog Input and Analog Output	5	-	0.5*	-	

ADDITIONAL APPLICATION CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	Limit 25°C	Unit
THD	Total Harmonic Distortion	V_C = V_{CC} , V_{IS} = 5 V R_L = 10 kΩ, f_{IS} =1 kHz sine wave	5	0.4	%
B_W	Maximum On-Channel Bandwidth or Minimum Frequency Response	C_L = 50 pF, t_r, t_f ≤ 20 ns R_L = 1 kΩ	5	40	MHz
f_1	Feedthrough Frequency	C_L = 50 pF, t_r, t_f ≤ 20 ns R_L = 1 kΩ	10	1	MHz
f_2	Signal Crosstalk Frequency	C_L = 50 pF, t_r, t_f ≤ 20 ns R_L = 1 kΩ	5	8	MHz
$V_{AO/I}$	Cross talk (Control Input to Signal Output)	R_L = 10 kΩ, t_r, t_f ≤ 20 ns V_C = 10 V	10	50	mV
fs	Maximum Control Input Repetition Rate	C_L = 50 pF, t_r, t_f ≤ 20 ns R_L = 1 kΩ	5 10 15	6 9 9.5	MHz

V_{CC} (V)	V_{IS} (V)	Switch Input I_{IS} (mA)			Switch Output, V_{OS} (V)	
		-55 °C	+25 °C	+125 °C	Min	Max
5 5	0 5	0.64 -0.64	0.51 -0.51	0.36 -0.36	- 4.6	0.4 -
10 10	0 10	1.6 -1.6	1.3 -1.3	0.9 -0.9	- 9.5	0.5 -
15 15	0 15	4.2 -4.2	3.4 -3.4	2.4 -2.4	- 13.5	1.5 -

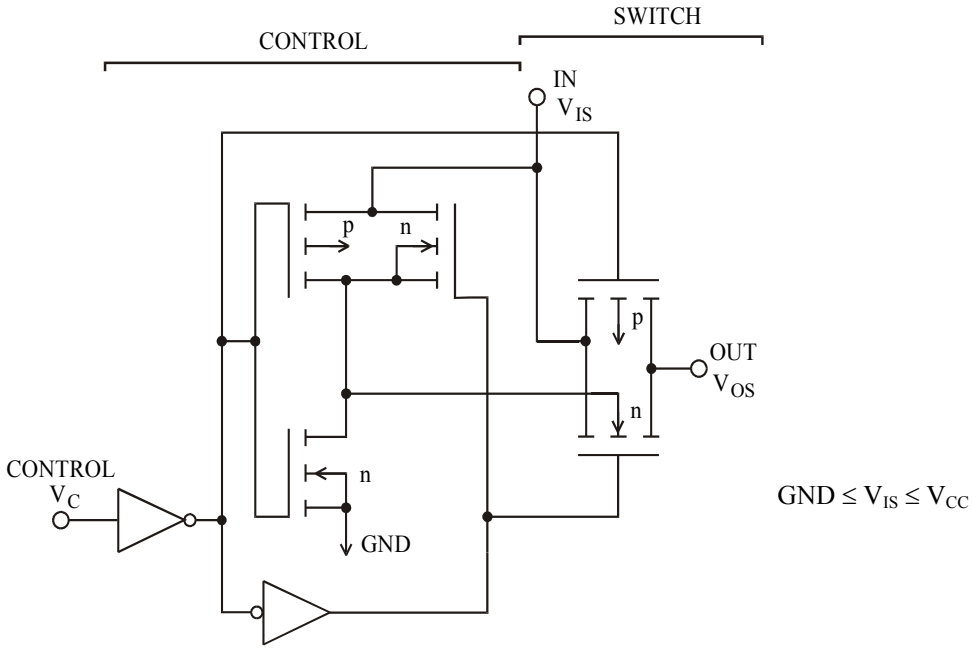


Figure 1. Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

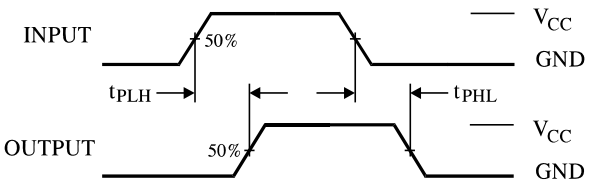


Figure 2. Switching Waveforms

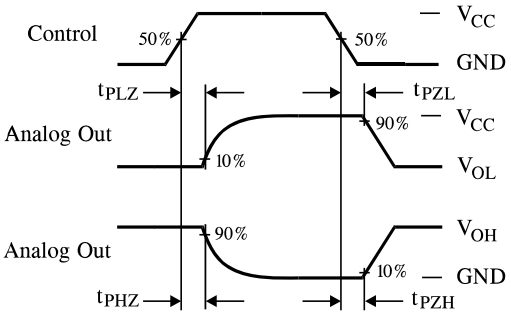
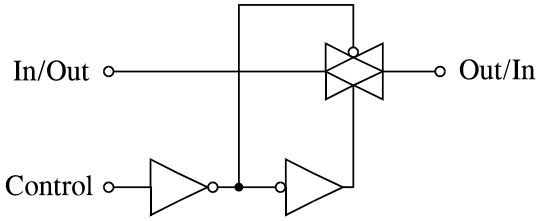


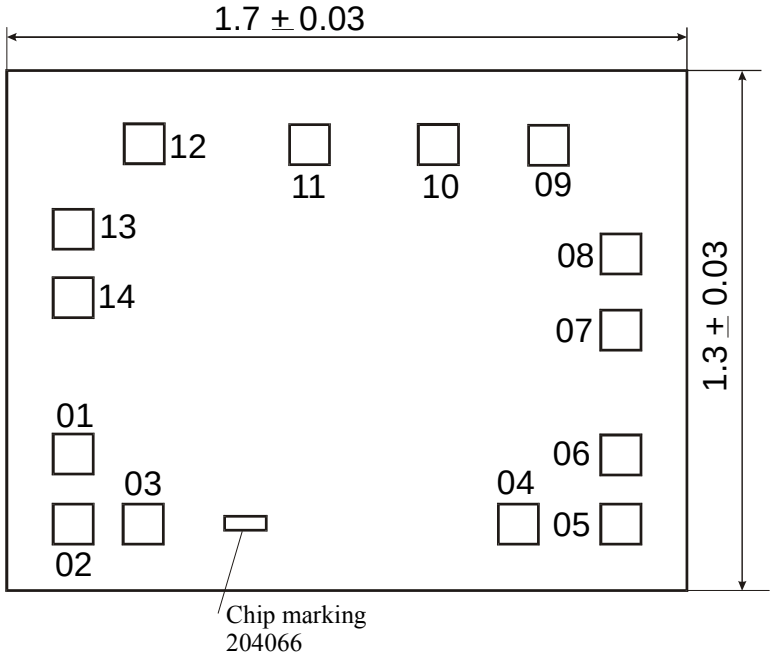
Figure 3. Switching Waveforms

EXPANDED LOGIC DIAGRAM
(1/4 of the Device)



Control	Switch
GND = L	OFF
V_{CC} = H	ON

CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x=0.740, y=0.147, right higher corner x=0.854, y=0.180
Chip thickness: 0.46±0.02mm

PAD LOCATION

Pad No	Pin No	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	01	0.116	0.289	0.110 x 0.110
02	02	0.116	0.116	0.110 x 0.110
03	03	0.291	0.116	0.110 x 0.110
04	04	1.229	0.116	0.110 x 0.110
05	05	1.485	0.116	0.110 x 0.110
06	06	1.485	0.291	0.110 x 0.110
07	07	1.485	0.601	0.110 x 0.110
08	08	1.485	0.792	0.110 x 0.110
09	09	1.304	1.063	0.110 x 0.110
10	10	1.029	1.063	0.110 x 0.110
11	11	0.707	1.063	0.110 x 0.110
12	12	0.291	1.063	0.110 x 0.110
13	13	0.116	0.853	0.110 x 0.110
14	14	0.116	0.681	0.110 x 0.110

Note: Pad location is given as per passivation layer