FEATURES

- CMOS LSI chips
- Connection with CPU
  Can be directly coupled with 80-port or 68-port system
- Available in chip form or in 100-pin plastic QFP
- Pin-to-Pin Replacement for SED1520 Series
- Many command set
- Total 80 (segment+common) drive sets
- Low power consumption - 30μW maximum at 2kHz external clock
- Power supply V_{DD} - V_{SS} : 2.4 to -5.5V
  V_{DD} - V_5 : 3.5 to -10.0V

DESCRIPTION

The IZ6570 family of dot matrix LCD (Liquid Crystal Display) drivers are designed for the display of characters and graphics.
The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.
The IZ6570 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.
These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.
The IZ6570 which is able to drive two lines of twelve characters each.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage (1)	V_{DD}	- 0.3 ~ 7.0	V
Supply Voltage (2)	$V_1 \sim V_5$	V_{DD} - 11.0 ~ V_{DD} + 0.3	V
Input Voltage	V_I	V_{SS} - 0.3 ~ 0.3	V
Power Dissipation	P_D	250	mW
Operating Temperature	T_a	- 20 ~ + 75	^oC
Storage Temperature	T_{stg}	- 55 ~ + 125	^oC

Notes:
1. All voltages are specified relative to V_{SS} = 0V.
2. The following relation must be always hold $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operating under these conditions is not implied.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{SS} = 0V, V_{DD} = 5V±10%)

Characteristic		Symbol	Condition	Applicable Terminals	Min	Typ	Max	Unit
Operating Voltage(1) Note 1	Recommended	V_{DD}		V_{DD}	4.5	5.0	5.5	V
	Available				2.4		5.5	
Operating Voltage(2)	Recommended	V_5		V_5	V_{DD} -10.0		V_{DD} -3.5	V
	Available				-13.0			
	Available	V_1, V_2	V_{LCD}= V_{DD}- V_5	V_1, V_2	V_{DD} -0.6V_{LCD}		V_{DD}	
	Available	V_3, V_4		V_3, V_4	V_5		V_{DD} -0.4V_{LCD}	
HIGH Input Voltage		V_{IH}		A0,Di, E, R/W, CS	2.0		V_{DD}	V
				CL, FR, M/S, RES	0.8 V_{DD}		V_{DD}	
LOW Input Voltage		V_{IL}		A0, Di, E, R/W, CS	V_{SS}		0.8	V
				CL, FR, M/S, RES	V_{SS}		0.2V_{DD}	
HIGH Output Voltage		V_{OH}	I_{OH} = -3.0 mA	D0 ÷ D7	2.4			V
			I_{OH} = -2.0 mA	FR	2.4			
			I_{OH} = -120 µA	OSC2	0.8 V_{DD}			
LOW Output Voltage		V_{OL}	I_{OL} = 3.0 mA	D0 ÷ D7			0.4	V
			I_{OL} = 2.0 mA	FR			0.4	
			I_{OL} = 120µA	OSC2			0.2V_{DD}	
Input Leakage Current		I_{LI}		A0, E, R/W, CS, CL, M/S, RES	-1.0		1.0	µA
Output Leakage Current		I_{LO}	Outputs are high impedance	D0 ÷ D7, FR	-3.0		3.0	µA
LCD Driver ON Resistance Note 2		R_{ON}	V_5= V_{DD} -5.0V	SEG0 ~ SEG79 COM0 ~ COM15		5.0	7.5	KΩ
Supply Current, Static		I_{DDQ}	CS = CL = V_{DD}	V_{DD}		0.05	1.0	µA
Supply Current, Dynamic		I_{DD}	f_{CL}=18kHz, V_{DD}=5.5V	V_{DD}		9.5	15.0	µA
			f_{cyc}=200kHz, V_{DD}=5.5V			300	500	
Oscillator Frequency		f_{OSC}	R_f =1MΩ±2%		15	18	21	KHz
Reset Time		t_R		RES	1.0		1000	µs

Notes: 1. Operating over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.

2. For a voltage differential of 0.1V between input (V_1, V_2, V_3, V_4) and output (COM, SEC) pins. All voltages within specified operating voltage range.

($Ta = 25^oC$, $V_{SS} = 0V$, $V_{DD} = 2.4 \sim 3.3V$)

Characteristic		Symbol	Condition	Applicable Terminals	Min	Typ	Max	Unit
Operating Voltage(1)	Recommended	V_{DD}		V_{DD}	2.4	3.0	3.3	V
Operating Voltage(2)	Recommended	V_5		V_5	V_{DD} -10.0		V_{DD} -3.5	V
	Available				V_{DD} -10.0			
	Available	V_1, V_2	$V_{LCD}= V_{DD}- V_5$	V_1, V_2	V_{DD} -0.6V_{LCD}		V_{DD}	
	Available	V_3, V_4		V_3, V_4	V_5		V_{DD} -0.4V_{LCD}	
HIGH Input Voltage		V_{IH}		A0,Di, E, R/W, CS	0.8 V_{DD}		V_{DD}	V
				CL, FR, M/S, RES	0.8 V_{DD}		0V_{DD}	
LOW Input Voltage		V_{IL}		A0, Di, E, R/W, CS	V_{SS}		0.2V_{DD}	V
				CL, FR, M/S, RES	V_{SS}		0.2V_{DD}	
HIGH Output Voltage		V_{OH}	I_{OH} = -500 µA	D0 ÷ D7	0.8 V_{DD}			V
			I_{OH} = -500 µA	FR	0.8 V_{DD}			
			I_{OH} = -50 µA	OSC2	0.8 V_{DD}			
LOW Output Voltage		V_{OL}	I_{OL} = 500 µA	D0 ÷ D7			0.2V_{DD}	V
			I_{OL} = 500 µA	FR			0.2V_{DD}	
			I_{OL} = 50µA	OSC2			0.2V_{DD}	
Input Leakage Current		I_{LI}		A0, E, R/W, CS, CL, M/S, RES	-1.0		1.0	µA
Output Leakage Current		I_{LO}	Outputs are high impedance	D0 ÷ D7, FR	-3.0		3.0	µA
LCD Driver ON Resistance Note 2		R_{ON}	V_5= 0V	SEG0 ~ SEG79 COM0 ~ COM15		10.0	50.0	KΩ
Supply Current, Static		I_{DDQ}	CS=CL=V_{DD}	V_{DD}		0.05	1.0	µA
Supply Current, Dynamic		I_{DD}	f_{CL}=18kHz, V_{DD}=5.5V	V_{DD}		6.0	12.0	µA
			f_{cyc}=200kHz, V_{DD}=5.5V			300	500	
Oscillator Frequency		f_{OSC}	R_f =1MΩ±2%		11	18	21	KHz
Reset Time		t_R		RES	1.0		1000	µs

Notes: 1. Operating over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.

2. For a voltage differential of 0.1V between input (V_1, V_2, V_3, V_4) and output (COM, SEC) pins. All voltages within specified operating voltage range.

TERMINAL DESCRIPTION

Terminal Name	Function
D0 ÷ D7	Data I/O
A0	Select display data or functions. HIGH: Display data LOW : Instructions
$\overline{RES}$	Resets the system and selects the interface type for a 68-port/80-port MPU HIGH: 68-port MPU interface LOW : 80-port MPU interface
$\overline{CS}$	Input. Active low. Effective for an external clock operation model only.
OSC1	Chip Select input LOW : Active level sensing
E $\overline{(RD)}$	Read/Write Enable signal when a 68-port MPU is connected. (Active LOW Read Enable signal when an 80-port MPU is connected)
R/W $\overline{(WR)}$	Read/Write Select signal when a 68-port MPU is connected. HIGH: Read Select LOW : Write Select (Active LOW Write Enable input when an 80-port MPU is connected Rising edge sensing)
$\overline{CL}$	Input. Effective for an external clock operation model only.
OSC2	External clock input (only effective with external clock types)
FR	LCD Frame (AC- conversion) signal input/output
SEGn	Segment output for driving the LCD
COMn	Common output for driving the LCD
M/S	Master/Slave Select signal
V_{DD}	5V power supply
V_{SS}	0V power supply (GND level)
V_1, V_2, V_3, V_4, V_5	Power supplies for driving the LCD. $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$

DISPLAY COMMANDS

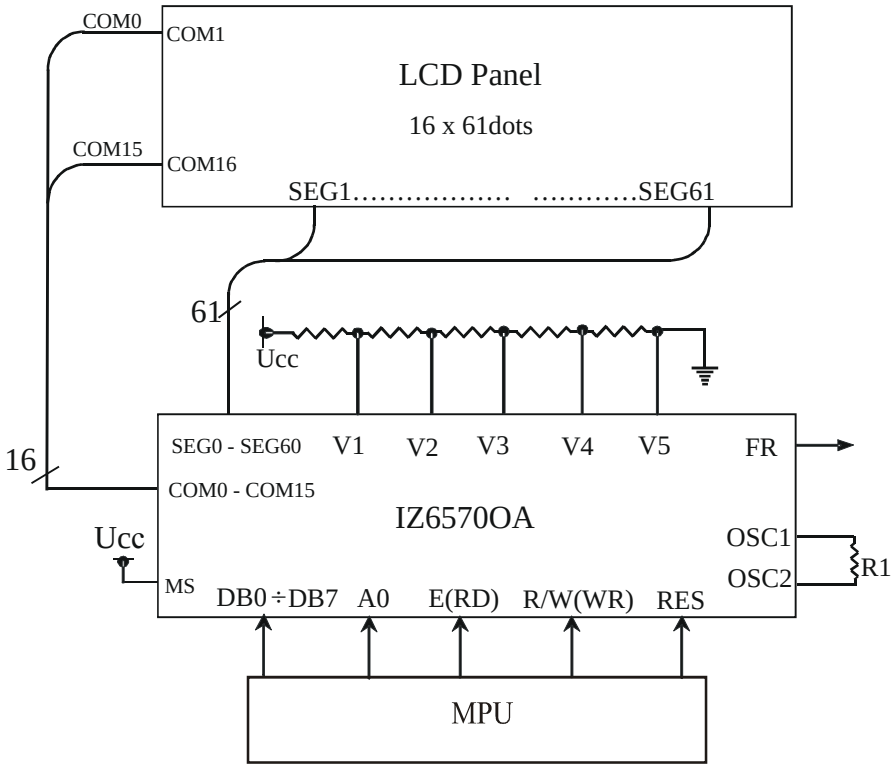
(Based on the 80-port MPU; the RD and WR commands differ for the 68-port MPU)

Command	Code											Description	
	RD	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0		
Display ON/OFF	1	0	0	1	0	1	0	1	1	1	0/1	Switches the entire display ON or OFF regardless of the Display RAM's data or the internal status. *Note	
Display START Line	1	0	0	1	1	0	Display START address (0 ÷ 31)					Determines the line of RAM data to be displayed at the display's top line (COM0)	
Page Address Set	1	0	0	1	0	1	1	1	0	Page (0 ÷ 3)		Sets the page of the Display RAM in the page address register	
Column (Segment) Address Set	1	0	0	0	Column address (0 ÷ 79)							Sets the column address of the Display RAM in the column address register	
Status Read	0	1	0	BUSY	ADC	ON/OFF	RESET	0	0	0	0	Reads the status. BUSY 1: Working 0: Ready ADC 1: Clockwise output 0: Counter clockwise ON/OFF 1: Display OFF 0: Display ON RESET 1: Reset 0: Normal	
Write Display Data	1	0	1	Write Data								Write the data to the Display Data RAM	These commands access a previously specified address of the Display RAM, after which the column address is incremented one
Read Display Data	0	1	1	Read Data								Read the data from the Display Data RAM	
ADC Select	1	0	0	1	0	1	0	0	0	0	0/1	Used to reverse the correspondence between the Display RAM's column addresses and segment driver output ports 0: Rightward (forward) output 1: Leftward (reverse)	
Static Drive ON/OFF	1	0	0	1	0	1	0	0	1	0	0/1	Selects normal display operation or static all-fit drive display operation 1: Static drive (Power Save) 0: Normal display	
Duty Select	1	0	0	1	0	1	0	1	0	0	0/1	Selects the duty factor for driving LCD cells 1: 1/32 duty 0: 1/16 duty	
Read Modify Write	1	0	0	1	1	1	0	0	0	0	0	Increments the column address counter by one only when display data is written but not when it is read	
End	1	0	0	1	1	1	0	1	1	1	0	Cancels the Ready Modify Write mode	
Reset	1	0	0	1	1	1	0	0	0	1	0	Resets the Display START line to the 1-st line in the register. Resets the column address counter and page address register to 0.	

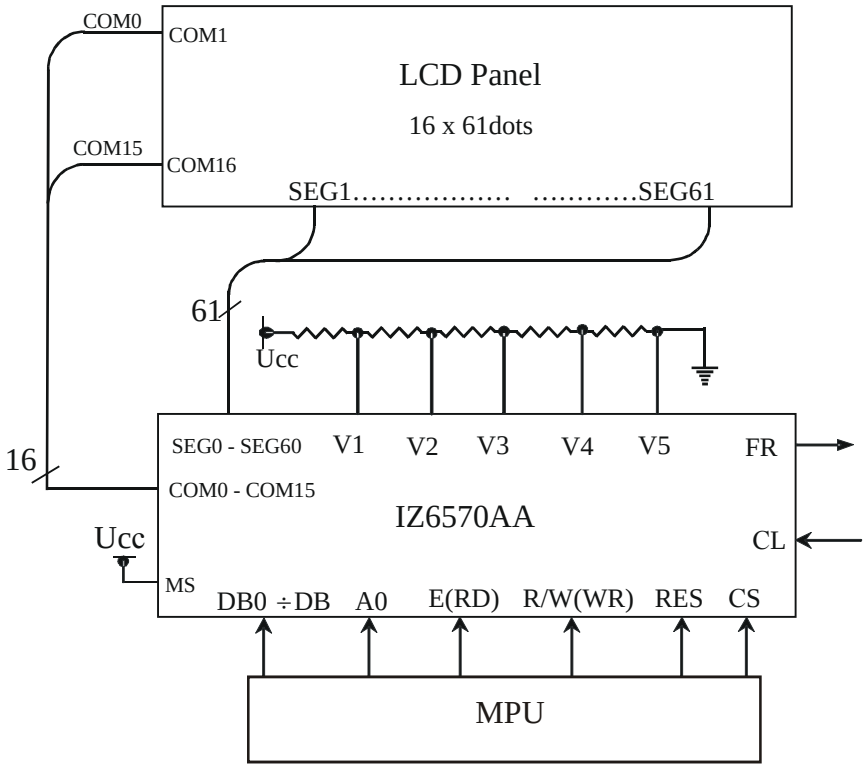
Note: Power Save mode is entered by selecting static drive in the Display OFF status

APLICATION CIRCUIT

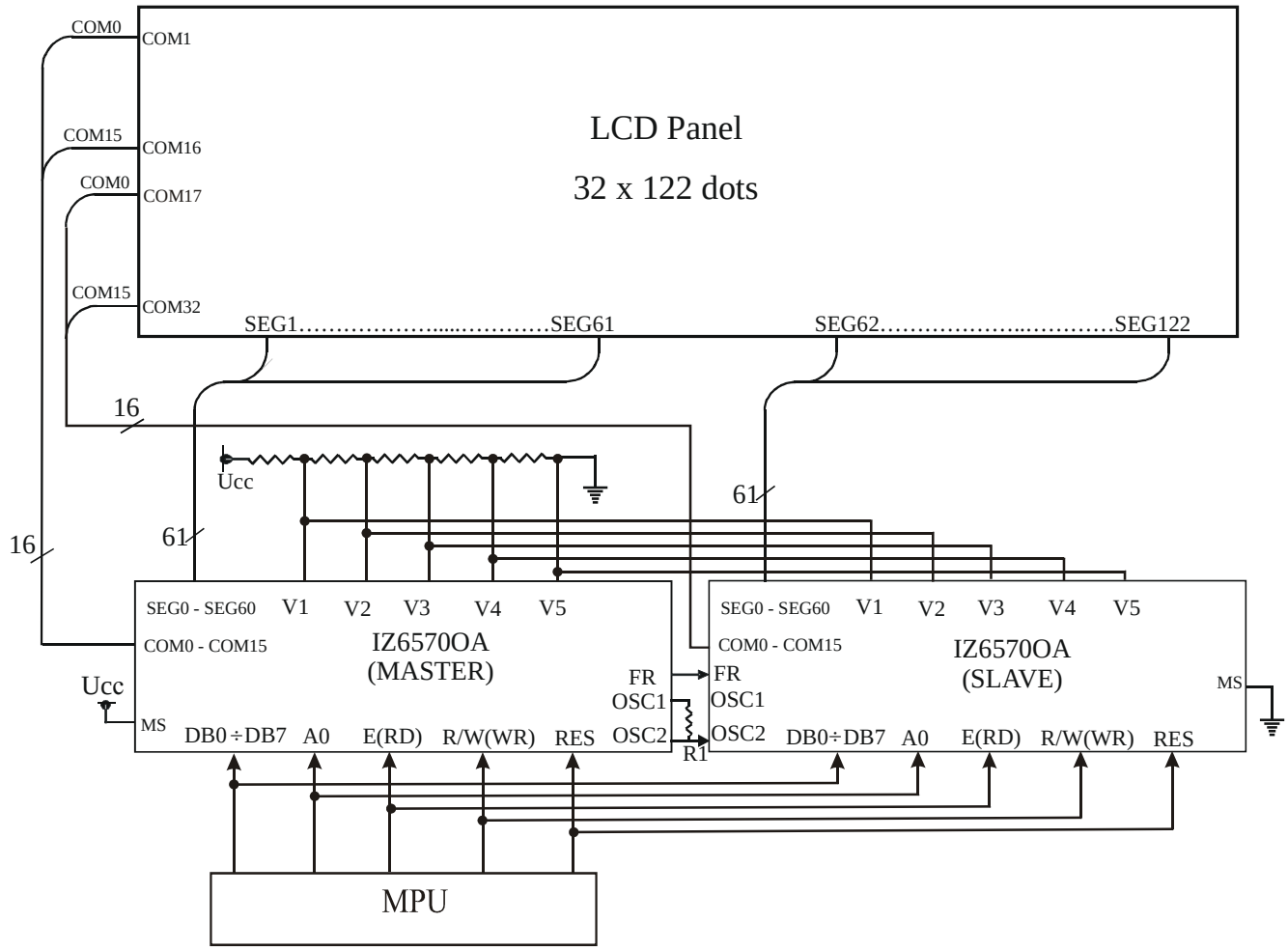
- **16 x 61 dots for IZ6570OA**



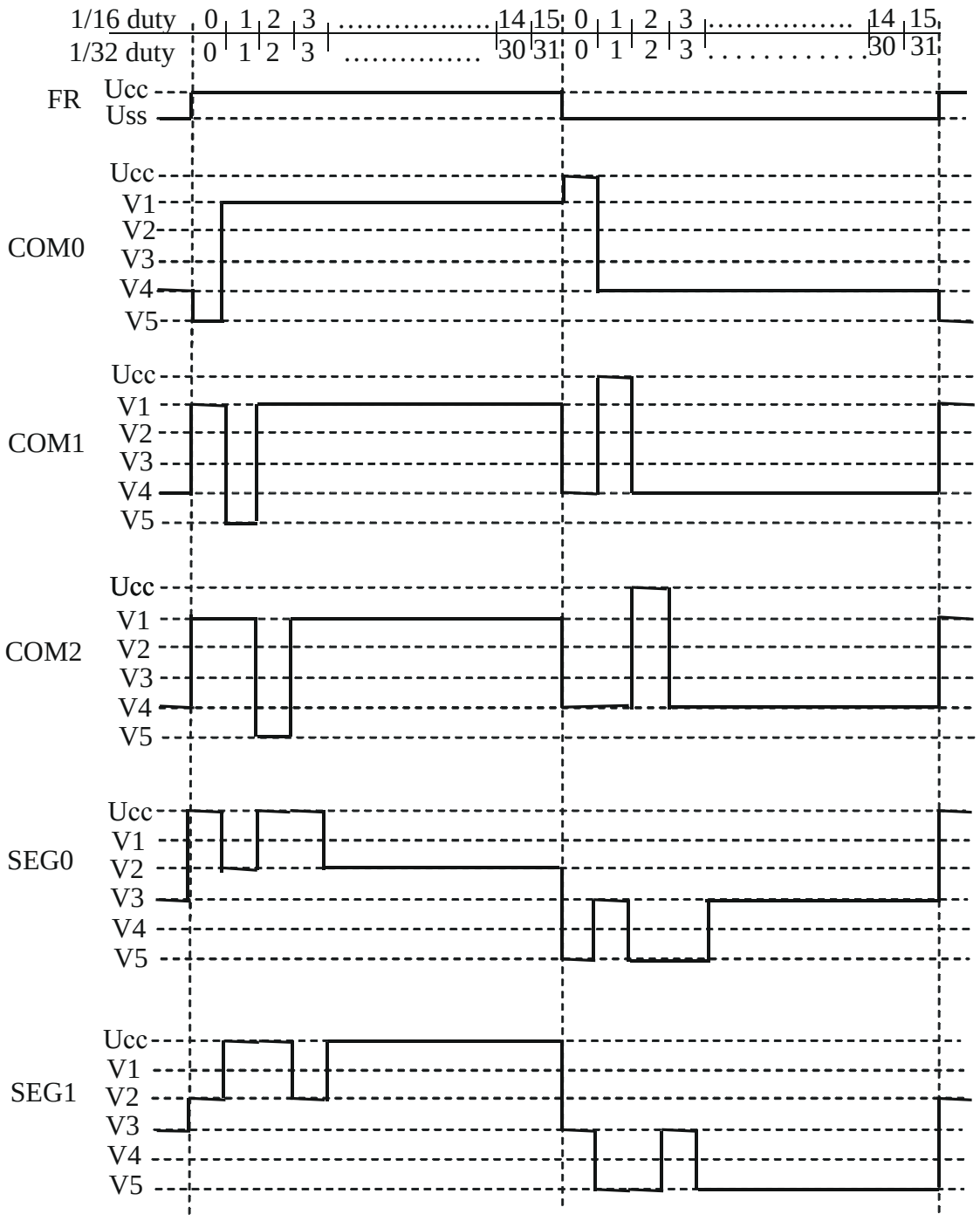
- **16 x 61 dots for IZ6570AA**



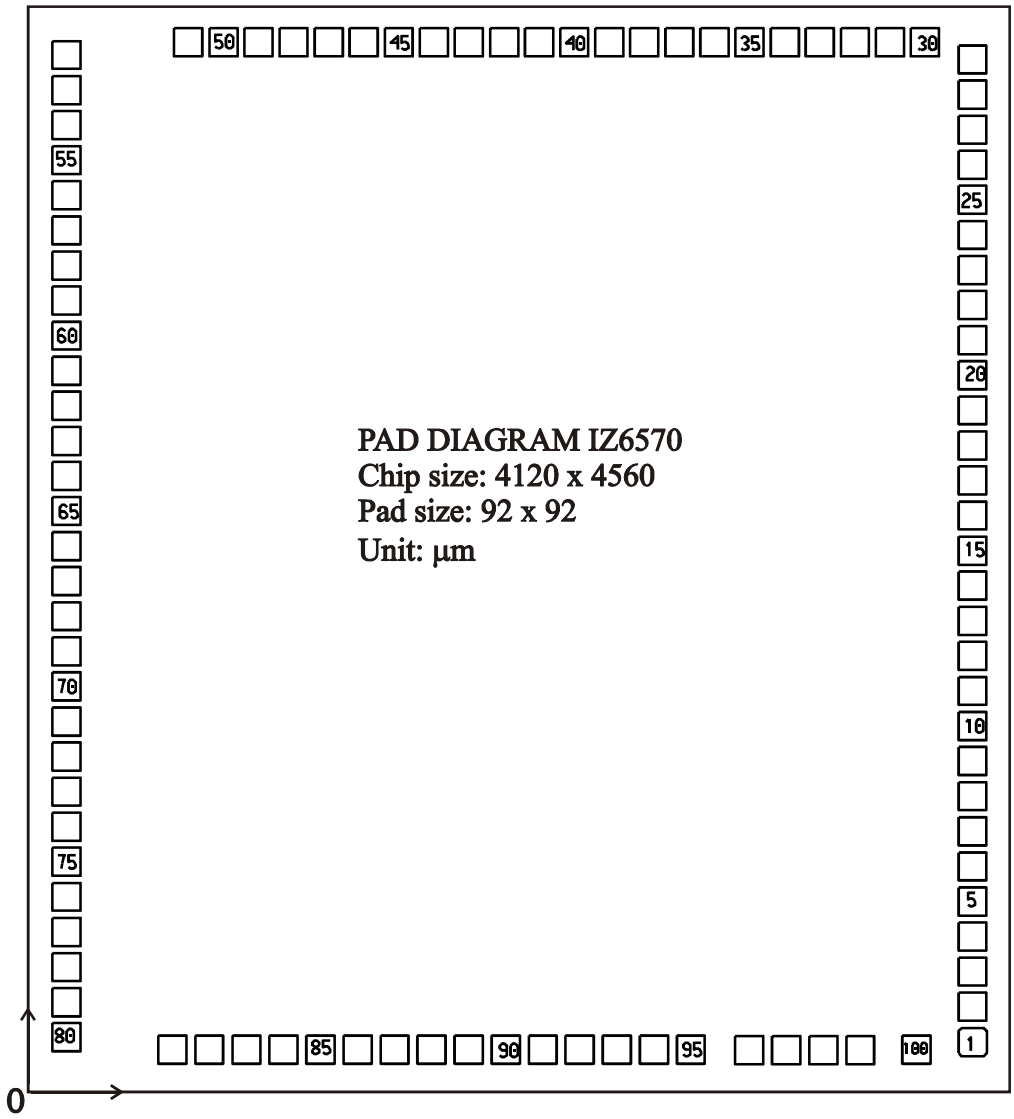
- **32 x 122 dots for IZ6570OA**



LCD Driving Waveform



PAD LOCATION



Note: STEP by PAD 150 µm;
pad size in a layer of pad window.

PAD COORDINATES

(Unit: μm)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	SEG71	3918	101	35	SEG37	2933	4359	69	SEG3	102	1751
2	SEG70	3918	251	36	SEG36	2783	4359	70	SEG2	102	1601
3	SEG69	3918	401	37	SEG35	2633	4359	71	SEG1	102	1451
4	SEG68	3918	551	38	SEG34	2483	4359	72	SEG0	102	1301
5	SEG67	3918	701	39	SEG33	2333	4359	73	A0	102	1151
6	SEG66	3918	851	40	SEG32	2183	4359	74	$\overline{CS}$	102	1001
7	SEG65	3918	901	41	SEG31	2033	4359	75	CL	102	851
8	SEG64	3918	1151	42	SEG30	1883	4359	76	E RD	102	701
9	SEG63	3918	1301	43	SEG29	1733	4359	77	R/W (WR)	102	551
10	SEG62	3918	1451	44	SEG28	1583	4359	78	GND	102	401
11	SEG61	3918	1601	45	SEG27	1433	4359	79	DB0	102	251
12	SEG60	3918	1751	46	SEG26	1283	4359	80	DB1	102	101
13	SEG59	3918	1901	47	SEG25	1133	4359	81	DB2	597	101
14	SEG58	3918	2051	48	SEG24	983	4359	82	DB3	747	101
15	SEG57	3918	2201	49	SEG23	833	4359	83	DB4	897	101
16	SEG56	3918	2351	50	SEG22	683	4359	84	DB5	1047	101
17	SEG55	3918	2501	51	SEG21	533	4359	85	DB6	1197	101
18	SEG54	3918	2651	52	SEG20	102	4301	86	DB7	1347	101
19	SEG53	3918	2801	53	SEG19	102	4151	87	V_{CC}	1498	101
20	SEG52	3918	2951	54	SEG18	102	4001	88	RES	1648	101
21	SEG51	3918	3101	55	SEG17	102	3851	89	FR	1798	101
22	SEG50	3918	3251	56	SEG16	102	3701	90	V5	1948	101
23	SEG49	3918	3401	57	SEG15	102	3551	91	V3	2122	101
24	SEG48	3918	3551	58	SEG14	102	3401	92	V2	2272	101
25	SEG47	3918	3701	59	SEG13	102	3251	93	SEG79	2422	101
26	SEG46	3918	3851	60	SEG12	102	3101	94	SEG78	2572	101
27	SEG45	3918	4001	61	SEG11	102	2351	95	SEG77	2722	101
28	SEG44	3918	4151	62	SEG10	102	2801	96	SEG76	2977	101
29	SEG43	3918	4301	63	SEG9	102	2651	97	SEG75	3127	101
30	SEG42	3683	4359	64	SEG8	102	2501	98	SEG74	3277	101
31	SEG41	3533	4359	65	SEG7	102	2351	99	SEG73	3432	101
32	SEG40	3383	4359	66	SEG6	102	2201	100	SEG72	3650	101
33	SEG39	3233	4359	67	SEG5	102	2051				
34	SEG38	3083	4359	68	SEG4	102	1901				

Note: Pads 74,75 are OSC1, OSC2 for $IZ6570_{OA}$ and CS, CL for $IZ6570_{AA}$ respectively. All other pad names are identical.