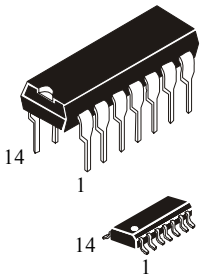
IW4006B

CMOS 18-Stage
Static Shift Register

The RCA-4006B types are composed of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tar at the fourth stage. Each section has an independent single-rail data path.

- Standardized, symmetrical output characteristics
- Operating Voltage Range: 3.0 to 18 V
- 100% tested for guiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range):
  1.0 V at V_{DD}=5.0 V
  2.0 V at V_{DD} =10.0 V
  2.5 V at V_{DD} =15.0 V



N SUFFIX
PLASTIC

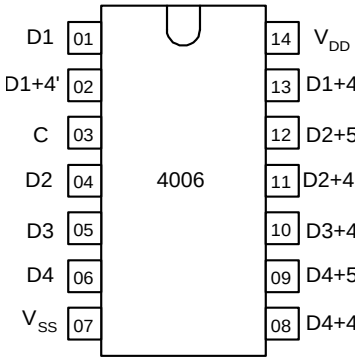
D SUFFIX
SOIC

ORDERING INFORMATION

IW4006BN Plastic
IW4006BD SOIC
IZ4006B Chip

T_A = -55° to 125° C for all packages

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
C	**D1**	**D2-D4**	**D1+4...D4+4**	**D1+4/**
⌊	L	L	L	Storage
⌊	H	H	H	Storage
⌈	X	X	Storage	D1
⌈	L	X	Storage	L
⌈	H	X	Storage	H
⌊	X	X	D1...D4	Storage

X = don't care

TERMINAL ASSIGNMENT

Pin.No	Symbol	Description
01	D1	Input Data
02	D1+4/	Output Data
03	C	Clock Data
04	D2	Input Data
05	D3	Input Data
06	D4	Input Data
07	V_{SS}	Ground
08	D4+4	Output Data
09	D4+5	Output Data
10	D3+4	Output Data
11	D2+4	Output Data
12	D2+5	Output Data
13	D1+4	Output Data
14	V_{DD}	Positive Pover Supply

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{DD} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP, SOIC Package	500**	mW
P_{tot}	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
**Derating: - Plastic DIP from -55 to +100°C
- SOIC Package from -55 to +65°C
- Plastic DIP: - 12 mW/°C from +100 to +125°C
- SOIC Package: : - 7 mW/°C from +65 to +125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}	DC Input Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation V_{IN} should be constrained to the range GND≤V_{IN} ≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either Vss or V_{DD}). Unused outputs must be left open.

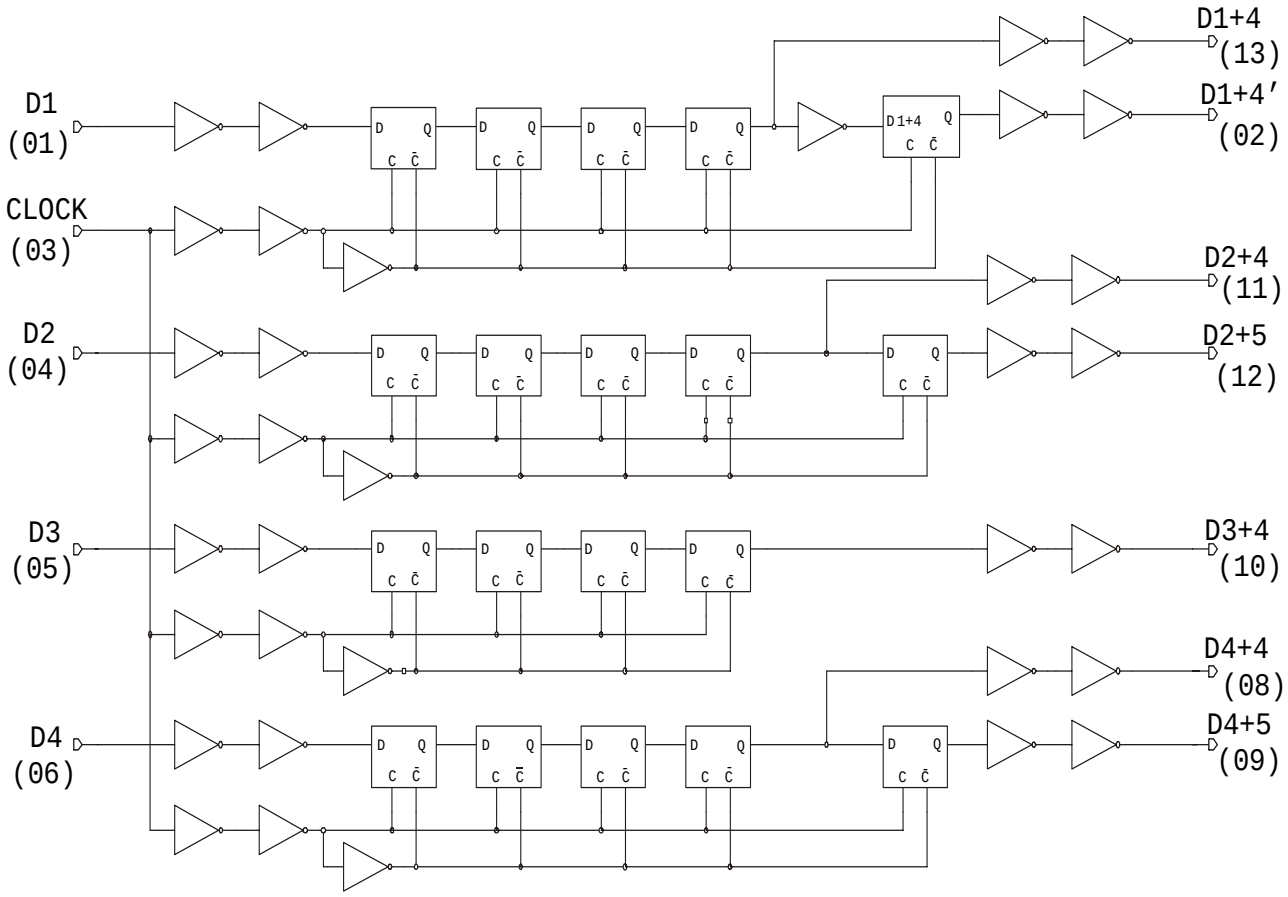
DC ELECTRICAL CHARACTERISTICS

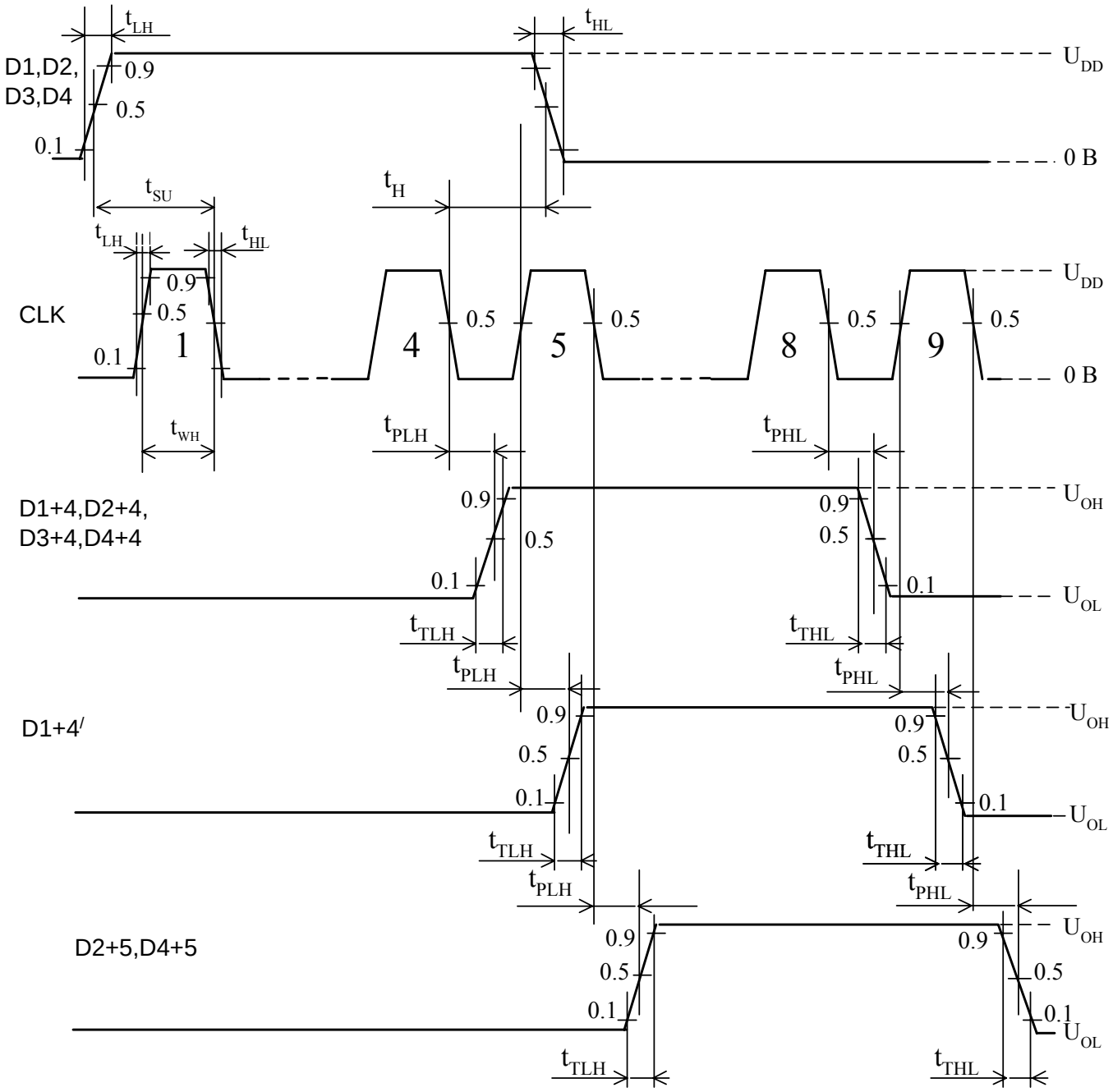
Symbol	Parameter	Test Conditions	V_{DD}, V	Guaranteed Limit						Unit
				55°C		125°C		25°C		
				min	max	min	max	min	max	
V_{IH}	Minimum High-Level Input Voltage	V_O = 0.5 V or V_{DD}-0.5 V	5.0	3.5	-	3.5	-	3.5	-	V
		V_O = 1.0 V or V_{DD}-1.0 V	10	7.0	-	7.0	-	7.0	-	
		V_O = 1.5 V or V_{DD}-1.5 V	15	11	-	11	-	11	-	
V_{IL}	Maximum Low - Level Input Voltage	V_O = 0.5 V or V_{DD}-0.5 V	5.0	-	1.5	-	1.5	-	1.5	V
		V_O = 1.0 V or V_{DD}-1.0 V	10	-	3.0	-	3.0	-	3.0	
		V_O = 1.5 V or V_{DD}-1.5 V	15	-	4.0	-	4.0	-	4.0	
V_{OH}	Minimum High-Level Output Voltage	V_I = V_{SS} или V_{DD}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	- - -	4.95 9.95 14.95	- - -	V
V_{OL}	Maximum Low-Level Output Voltage	V_I = V_{SS} или V_{DD}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0.05 0.05 0.05	- - -	0.05 0.05 0.05	V
I_{IL}	Maximum Input Current	V_I = V_{SS}	18	-	-0.1	-	-1.0	-	-0.1	µA
I_{IH}	Maximum Input Leakage Current	V_I = V_{DD}	18	-	+0.1	-	+1.0	-	+0.1	µA
I_{DD}	Maximum Quiescent Supply Current (per Package)	V_I = V_{SS} or V_{DD}	5.0 10 15 20	- - - -	5.0 10.0 20.0 100	- - - -	150 300 600 3000	- - - -	5.0 10 20 100	µA
I_{OL}	Minimum Output Low (Sink) Current	V_I = V_{SS} or V_{DD} V_{OL} = 0.4 V V_{OL} = 0.5 V V_{OL} = 1.5 V	 5.0 10 15	 0.64 1.6 4.2	 - - -	 0.36 0.9 2.4	 - - -	 0.51 1.3 3.4	 - - -	mA
I_{OH}	Minimum Output High (Source) Current	V_I = V_{SS} or V_{DD} V_{OH} = 2.5 V V_{OH} = 4.6 V V_{OH} = 9.5 V V_{OH} = 13.5 V	 5.0 5.0 10 15	 -2.0 -0.64 -1.6 -4.2	 - - - -	 -1.15 -0.36 -0.9 -2.4	 - - - -	 -1.6 -0.51 -1.3 -3.4	 - - - -	mA
C_{IN}	Maximum Input Capacitance		-	-	-	-	-	-	7.5	pF

TIMING REQUIREMENTS (C_L=50 пФ, R_L = 200 кОм, $t_{LH} = t_{HL} \leq 20$ нс)

Symbol	Parameter	U_{DD}, V	Guaranteed Limit						Unit
			55°C		125°C		25°C		
			min	max	min	max	min	max	
t_{PHL}, t_{PLH}	Propagation Delay Time	5.0	-	400	-	800	-	400	ns
		10		200		400		200	
		15		160		320		160	
t_{THL}, t_{TLH}	Transition Time	5.0	-	200	-	400	-	200	ns
		10		100		200		100	
		15		80		160		80	
t_{SU}	Minimum Data Setup Time	5.0	100	-	200	-	100	-	ns
		10	50		100		50		
		15	40		80		40		
t_H	Minimum Hold Time, Clock to Data	5.0	150	-	300	-	150	-	ns
		10	80		160		80		
		15	60		120		60		
tw	Minimum Clock Pulse Width	5.0	200	-	400	-	200	-	nc
		10	90		180		90		
		15	60		120		60		
f_C	Maximum Clock Input Freguency	5.0		2.5		1.25		2.5	MHz
		10		5.0		2.5		5.0	
		15		7.0		3.5		7.0	
$t_{r(CL)}$ $t_{f(CL)}$	Maximum Clock Input Rise or Fall Time	5.0		15		15		15	μs
		10		15		15		15	
		15		15		15		15	

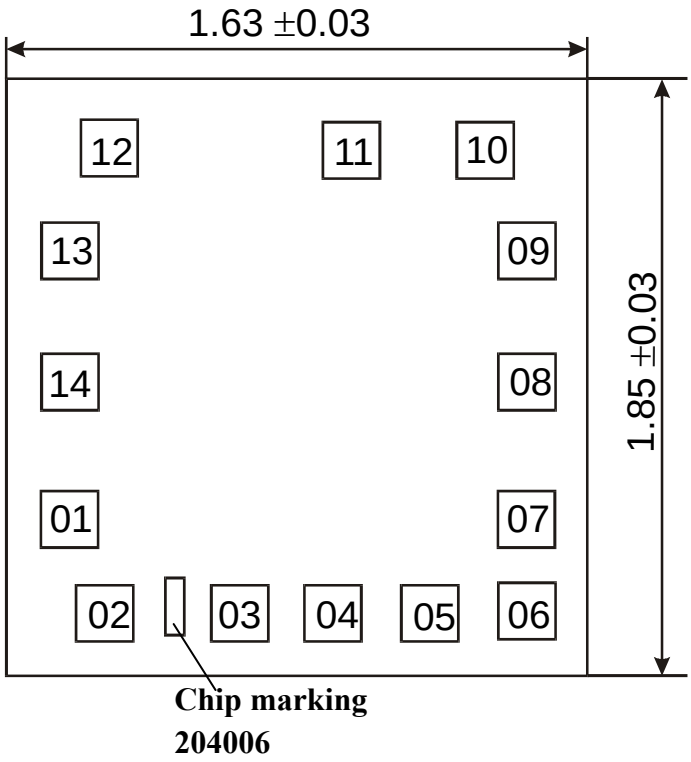
LOGIS DIAGRAM WITH DETAIL OF LATCH





SWITCHING WAVEFORMS

CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x = 0.630, y = 0.102;
Thickness of chip:0.46 ± 0.02 mm

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	D1	0.164	0.453	0.100 x 0.100
02	D1+4/	0.215	0.138	0.100 x 0.100
03	C	0.703	0.138	0.100 x 0.100
04	D2	0.960	0.138	0.100 x 0.100
05	D3	1.135	0.138	0.100 x 0.100
06	D4	1.394	0.138	0.100 x 0.100
07	V_{SS}	1.394	0.493	0.100 x 0.100
08	D4+4	1.394	0.918	0.100 x 0.100
09	D4+5	1.394	1.313	0.100 x 0.100
10	D3+4	1.354	1.606	0.100 x 0.100
11	D2+4	0.877	1.606	0.100 x 0.100
12	D2+5	0.215	1.606	0.100 x 0.100
13	D1+4	0.136	1.318	0.100 x 0.100
14	V_{DD}	0.164	0.784	0.100 x 0.100

Note: Location is given as per passivation layer