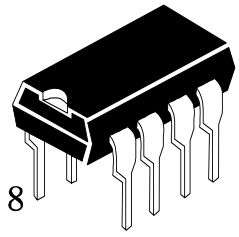
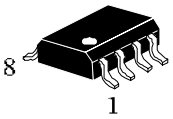
3.3 AND 5.0 VOLT MICROMONITOR

DESCRIPTION

The IN1708 3 or 5.0 Volt MicroMonitor monitors three vital conditions for a microprocessor power supply, voltage sense, and external override A precision temperature-compensated reference and comparator circuit monitors the status of Vcc at *ne device and at an upstream point for maximum protection When the sense input detectsan out-of-tolerance condition a non-maskable interrupt is generated As the voltage at the device degrades an internal power fail signal is generated which forces the reset to an active state When Vcc returns to an in-tolerance condition, the reset signal is kept in the active state for a minimum of 130 ms to allow the power supply and processor to stabilize The third function the IN1708 performs is pushbutton reset control The IN1708 debounces the pushbutton input and guarantees an active reset pulse width of 130 ms minimum



IN1708N - plastic DIP



IN1708D - SOIC

FEATURES

- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5%, 10% or 20% resets for 3.3V systems and

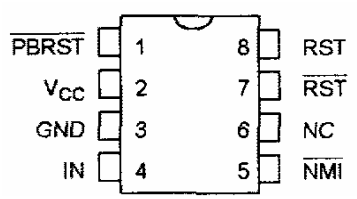
5% or 10% resets for 5.0V systems

- Eliminates the need for discrete components
- 20% tolerance compatible with 3 0 volt systems
- 8-pin DIP, 8-pin SOIC packages available
- Industrial temperature range —40°C to +85°C

INTEGRAL

PIN ASSIGNMENT

PIN	DESCRIPTION
$\overline{\text{PBRST}}$	Pushbutton Reset Input
Vcc	Power Supply
GND	Ground
IN	Input
$\overline{\text{NMI}}$	Non-maskable Interrupt
NC	No Connect
$\overline{\text{RST}}$	Active Low Reset Output
RST	Active High Reset Output



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Ground -0.5V to +7.0V
Voltage on I/O Relative to Ground -0 5V to V_{CC} +0.5V
Operating Temperature -40°C to +85°C
Storage Temperature -55°C to +125°C
Soldering Temperature 260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods of time may affect reliability

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2		5.5	V	1
$\overline{\text{PBRST}}$ Input High Level	V_{IH}	2.0 VCC-0.5		VCC+0.3	V	1, 3 1, 4
$\overline{\text{PBRST}}$ Input Low Level	V_{IL}	-0.03		+0.5	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C, V_{cc}=1 2V to 5 5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Trip Point IN1708	V_{CCTP}	4.25	4.40	4.50	V	1
Input Leakage	I_{IL}	-1.0		+1.0	µA	2
Output Current @ 2.4V	I_{OH}		350		µA	3
Output Current @ 0.4V	I_{OL}	10			mA	3
Output Voltage	V_{OH}		V_{CC}-0.1		V	3
Operating Current @ V_{CC} < 5.5V	I_{CC}			60	µA	5
Operating Current @ V_{CC} < 3.6V	I_{CC}			50	µA	5
IN Input Trip Point	V_{TP}	1.20	1.25	1.30	V	1

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PBRST = V_{IL}	t_{PB}	150			ns	
Reset Active Time	t_{RST}	130	205	285	ms	
V_{CC} Detect to RST and RST	t_{RPD}		5	8	µs	7
V_{CC} Slew Rate	t_F	20			µs	
V_{CC} Detect to RST and RST	t_{RPU}	130	205	285	ms	6
V_{CC} Slew Rate	t_R	0			ns	
PBRST Stable Low to RST and RST	t_{PDLY}			250	ns	
V_{IN} Detect to NMI	t_{IPD}		5	8	µs	7

OPERATION

Power Monitor

The IN1708 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure When V_{CC} falls below the minimum V_{CC} tolerance, a comparator outputs the RST and $\overline{RST}$ signals. RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moment of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 130 ms to allow the power supply and processor to stabilize/

Pushbutton Reset

The IN1708 provides an input pin for direct connection to a pushbutton reset (see Figure 2) The pushbutton reset input requires an active low signal Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 130ms minimum will be generated The 130ms delay commences as the pushbutton reset input is released from the low level The pushbutton can be initiated by connecting the NMI output to the $\overline{PBRST}$ input as shown in Figure 3

Non-Maskable Interrupt

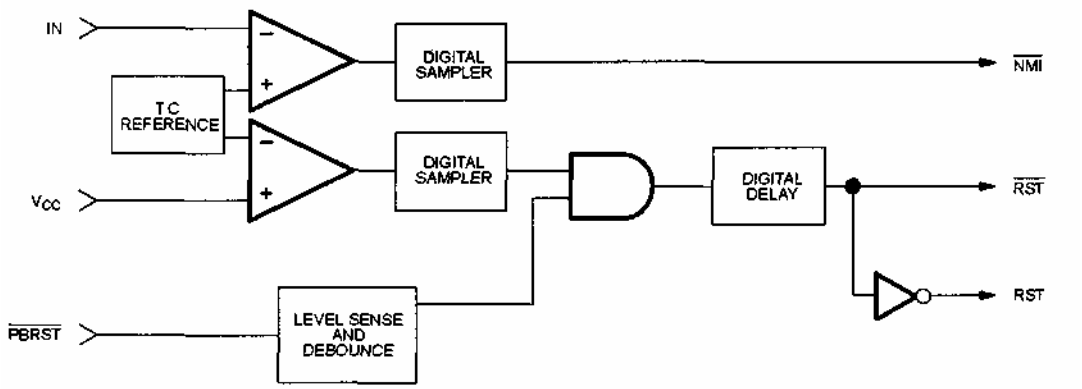
The IN1708 generates a non-maskable interrupt ($\overline{NMI}$) for early warning of a power failure A precision comparator monitors the voltage level at the IN pin relative to an on-chip reference generated by an internal band gap The IN pin is a high impedance input allowing for a user-defined sense point An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals This sense point may be derived from a regulated supply or from a higher DC voltage level closerto the mam system power input. Since the IN trip point V_{TP} is 1.25 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5 Proper operation of the IN1708 requires that the voltage at the IN pin be limited to V_{CC} Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 5 A simple approach to solving the equation is to select a value for R2 high enough to keep power consumption low, and solve for R1 The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for system shutdown between $\overline{NMI}$ and RST/$\overline{RST}$

When the supply being monitored decays to the voltage sense point, the IN1708 pulses the $\overline{NMI}$ output to the active state for a minimum 200 us The NMI power fail detection circuitry also has built-in hysteresis of 100uV. The supply must be below the voltage sense point for approximately 5 us before a low NMI will be generated In this way, power supply noise is removed from the monitoring function, preventing false interrupts During a power-up, any detected IN pin levels below V_{TP} by the comparator are disabled

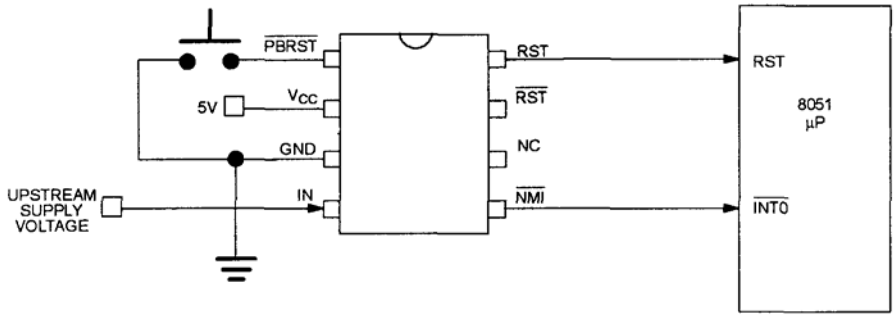
from generating an interrupt until V_{CC} r|ses to V_{CCTP} As a result, any potential NMI pulse will not be initiated until V_{CC} reaches V_{CCTP}

Connecting $\overline{NMI}$ to $\overline{PBRST}$ would allow the non-maskable interrupt to generate an automatic reset when an out-of-tolerance condition occurred in a monitored supply. An example is shown in Figure 3

MICROMONITOR BLOCK DIAGRAM Figure 1



PUSHBUTTON RESET Figure 2



PUSHBUTTON RESET CONTROLLED BY NMT Figure 3

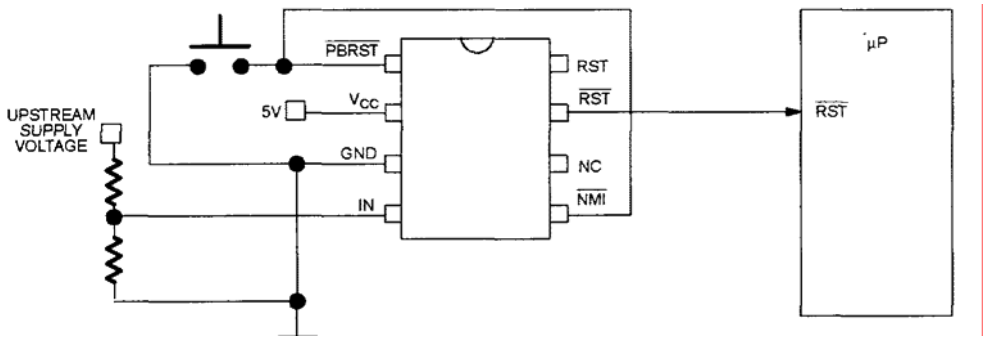


Fig. 4 TIMING DIAGRAM: PUSHBUTTON RESET

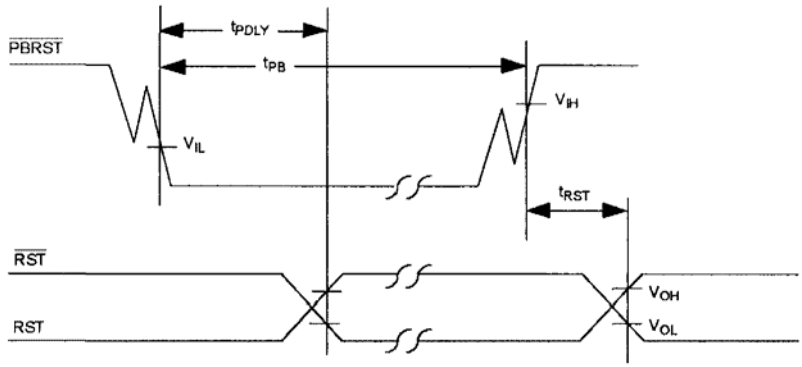


Fig. 5 NON-MASKABLE INTERRUPT CIRCUIT EXAMPLE

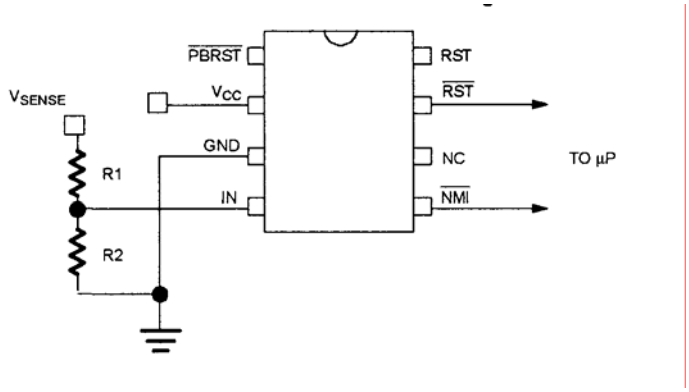


Fig. 6 TIMING DIAGRAM: NON-MASKABLE INTERRUPT

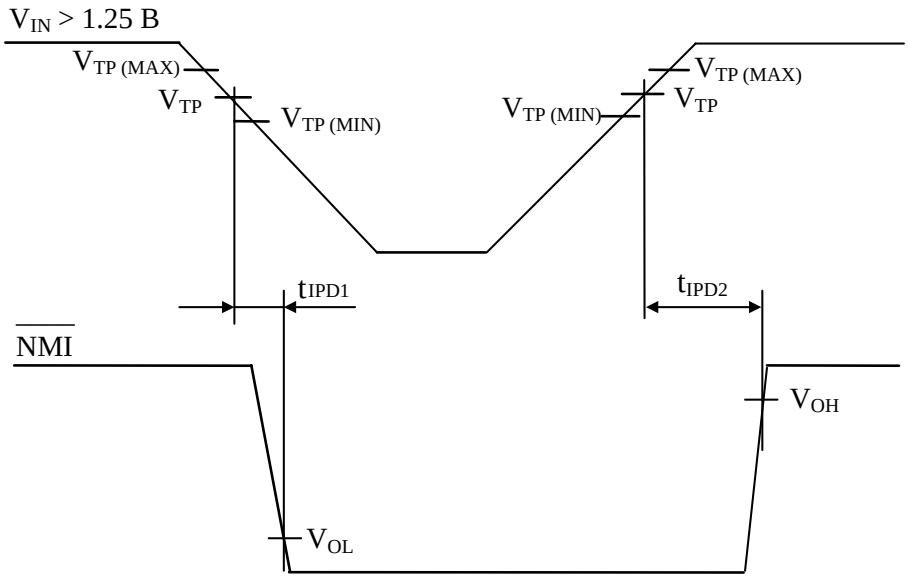


Fig. 7 TIMING DIAGRAM: POWER DOWN

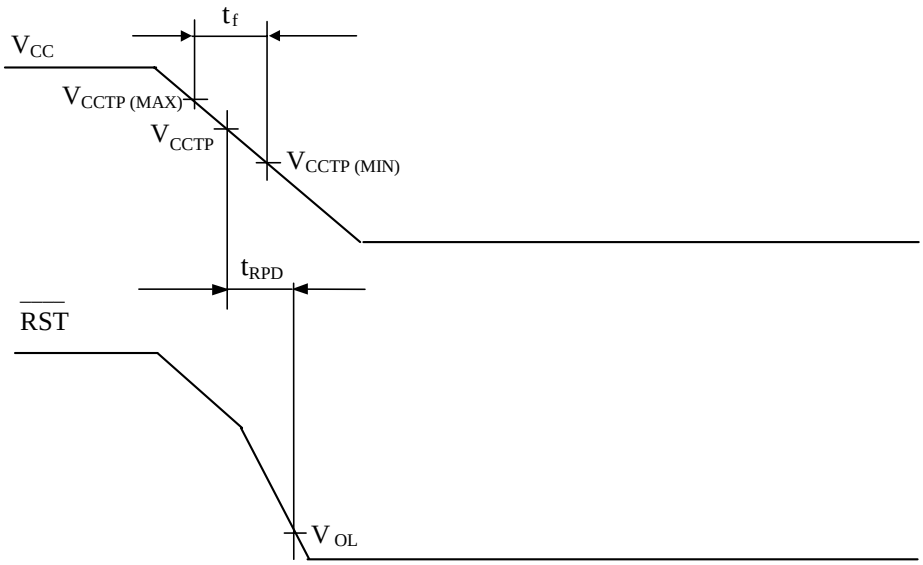


Fig. 8 TIMING DIAGRAM: POWER UP

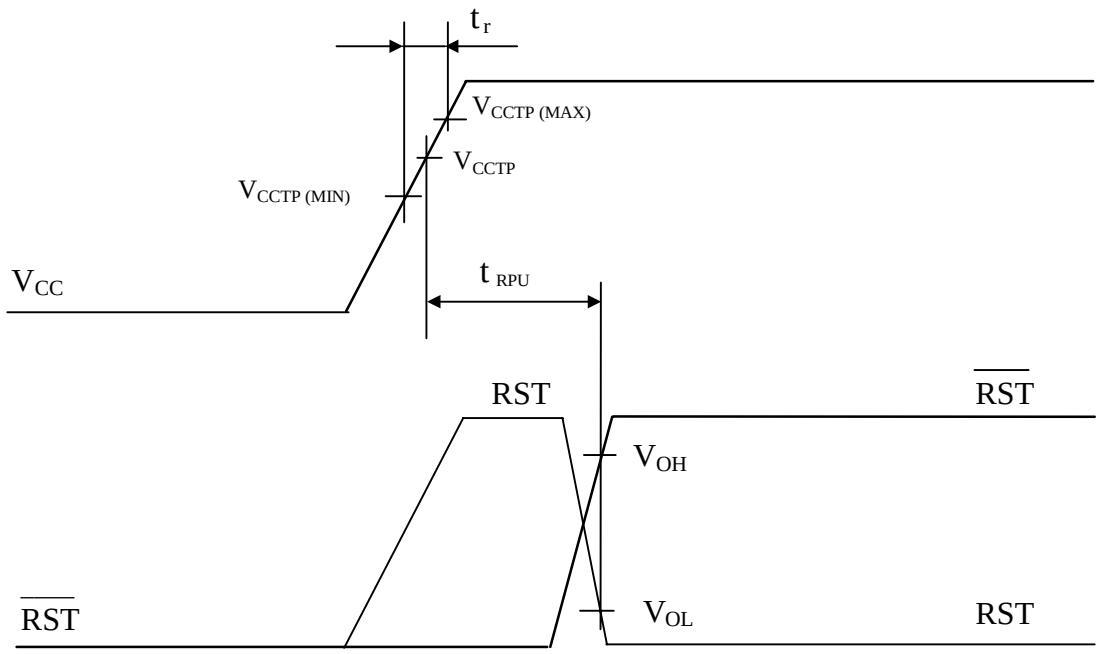
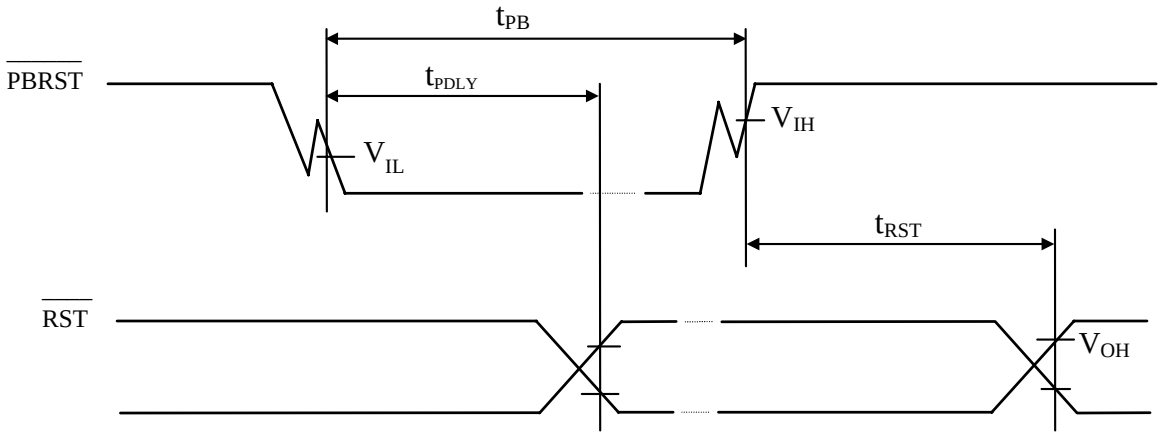
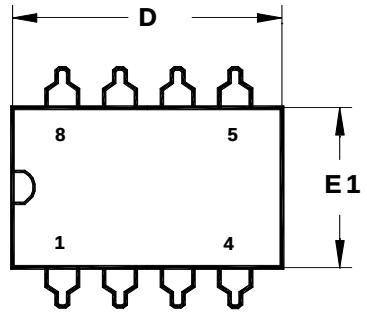
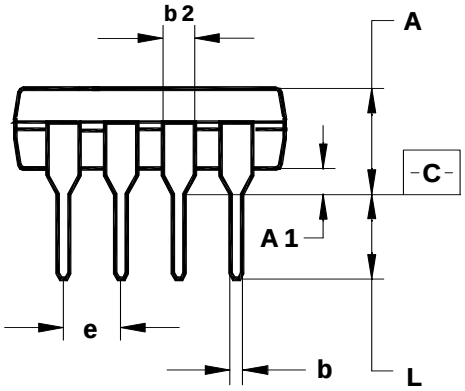


Fig. 9 TIMING DIAGRAM: PUSHBUTTON RESET

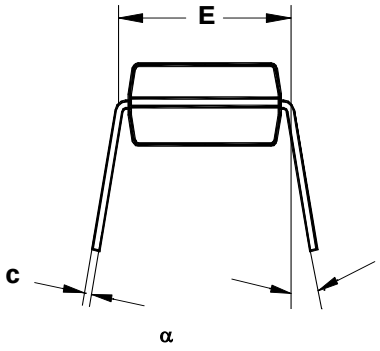


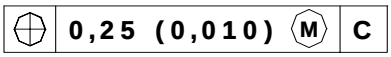
N SUFFIX PLASTIK DIP
(MS-001BA)





Mounting plate

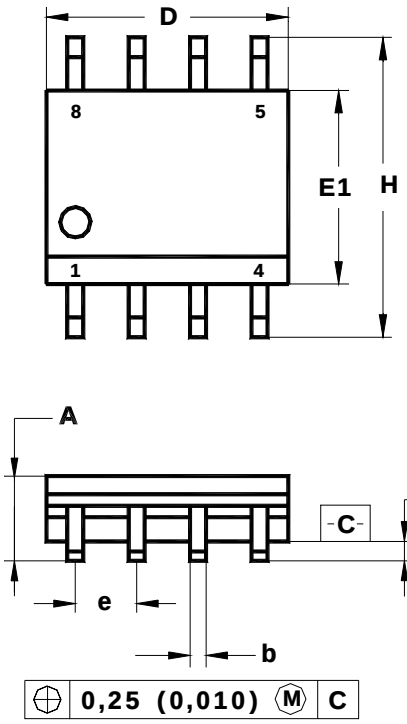




	D	E1	A	b	b2	e	α	L	E	c	A1
mm											
min	9.02	6.07	—	0.36	1.14		0°	2.93	7.62	0.20	0.38
max	10.16	7.11	5.33	0.56	1.78	2.54	15°	3.81	8.26	0.36	—
inches											
min	0.355	0.240	—	0.014	0.045		0°	0.115	0.300	0.008	0.015
max	0.400	0.280	0.210	0.022	0.070	0.1	15°	0.150	0.325	0.014	—

INTEGRAL

N SUFFIX PLASTIK SOP
(MS-012AA)



	D	E1	H	b	e	α	A	A1	c	L	h
mm											
min	4.80	3.80	5.80	0.33		0°	1.35	0.10	0.19	0.41	0.25
max	5.00	4.00	6.20	0.51	1.27	8°	1.75	0.25	0.25	1.27	0.50
inches											
min	0.1890	0.1497	0.2284	0.013		0°	0.0532	0.0040	0.0075	0.016	0.0099
max	0.1968	0.1574	0.2440	0.020	0.100	8°	0.0688	0.0090	0.0098	0.050	0.0196

INTEGRAL