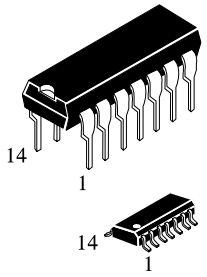
IW4093B

Quad 2-Input NAND Schmitt Triggers

High-Voltage Silicon-Gate CMOS

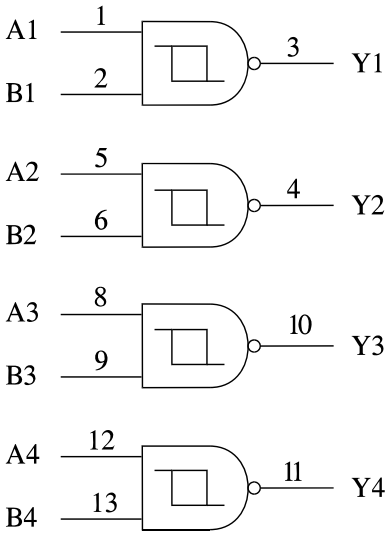


ORDERING INFORMATION
IW4093BN Plastic
IW4093BD SOIC
IZ4093B CHIP
T_A = -55° to 125° C for all packages

The IW4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative- going signals. The difference between the positive voltage (V_{+}) and the negative voltage (V_{-}) is defined as hysteresis voltage (V_H) (see Fig.1).

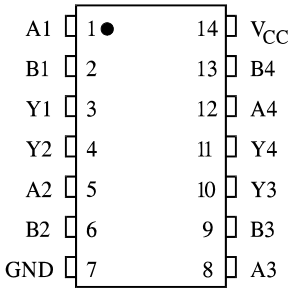
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  0.5 V min @ 5.0 V supply
  1.0 V min @ 10.0 V supply
  1.5 V min @ 15.0 V supply

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

L – LOW voltage level

H – HIGH voltage level

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	500 500	mW
Ptot	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 12 mW/°C from 100° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125 °C	
V_T+min	Minimum Positive-Going Input Threshold Voltage	Input on terminals A or B; other inputs to V_{CC}	5.0 10 15	2.2 4.6 6.8	2.2 4.6 6.8	2.2 4.6 6.8	V
		Input on terminals A and B; other inputs to V_{CC}	5.0 10 15	2.6 5.6 6.3	2.6 5.6 6.3	2.6 5.6 6.3	
V_T+max	Maximum Positive-Going Input Threshold Voltage	Input on terminals A or B; other inputs to V_{CC}	5.0 10 15	3.6 7.1 10.8	3.6 7.1 10.8	3.6 7.1 10.8	V
		Input on terminals A and B; other inputs to V_{CC}	5.0 10 15	4 8.2 12.7	4 8.2 12.7	4 8.2 12.7	
V_T-min	Minimum Negative-Going Input Threshold Voltage	Input on terminals A or B; other inputs to V_{CC}	5.0 10 15	0.9 2.5 4	0.9 2.5 4	0.9 2.5 4	V
		Input on terminals A and B; other inputs to V_{CC}	5.0 10 15	1.4 3.4 4.8	1.4 3.4 4.8	1.4 3.4 4.8	
V_T-max	Maximum Negative-Going Input Threshold Voltage	Input on terminals A or B; other inputs to V_{CC}	5.0 10 15	2.8 5.2 7.4	2.8 5.2 7.4	2.8 5.2 7.4	V
		Input on terminals A and B; other inputs to V_{CC}	5.0 10 15	3.2 6.6 9.6	3.2 6.6 9.6	3.2 6.6 9.6	
$V_H$min Note	Minimum Hysteresis Voltage	Input on terminals A or B; other inputs to V_{CC}	5.0 10 15	0.3 1.2 1.6	0.3 1.2 1.6	0.3 1.2 1.6	V
		Input on terminals A and B; other inputs to V_{CC}	5.0 10 15	0.3 1.2 1.6	0.3 1.2 1.6	0.3 1.2 1.6	
$V_H$max Note	Maximum Hysteresis Voltage	Input on terminals A or B; other inputs to V_{CC}	5.0 10 15	1.6 3.4 5	1.6 3.4 5	1.6 3.4 5	V
		Input on terminals A and B; other inputs to V_{CC}	5.0 10 15	1.6 3.4 5	1.6 3.4 5	1.6 3.4 5	
I_{IN}	Maximum Input Leakage Current	V_{IN} = GND or V_{CC}	18	±0.1	±0.1	±1.0	µA

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND) - continued

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125 °C	Unit
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0 10 15 20	1 2 4 20	1 2 4 20	30 60 120 600	μA
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC} U_{OL}=0.4 V U_{OL}=0.5 V U_{OL}=1.5 V	 5.0 10 15	 0.64 1.6 4.2	 0.51 1.3 3.4	 0.36 0.9 2.4	mA
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC} U_{OH}=2.5 V U_{OH}=4.6 V U_{OH}=9.5 V U_{OH}=13.5 V	 5.0 5.0 10 15	 -2.0 -0.64 -1.6 -4.2	 -1.6 -0.51 -1.3 -3.4	 -1.15 -0.36 -0.9 -2.4	mA
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= V_{CC}	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V

Note. $V_H$min > (V_{T+}min)-(V_{T-}max); $V_H$max = (V_{T+}max) + (V_{T-}min).

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=200kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figure 2)	5.0 10 15	380 180 130	380 180 130	760 360 260	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figure 2)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF

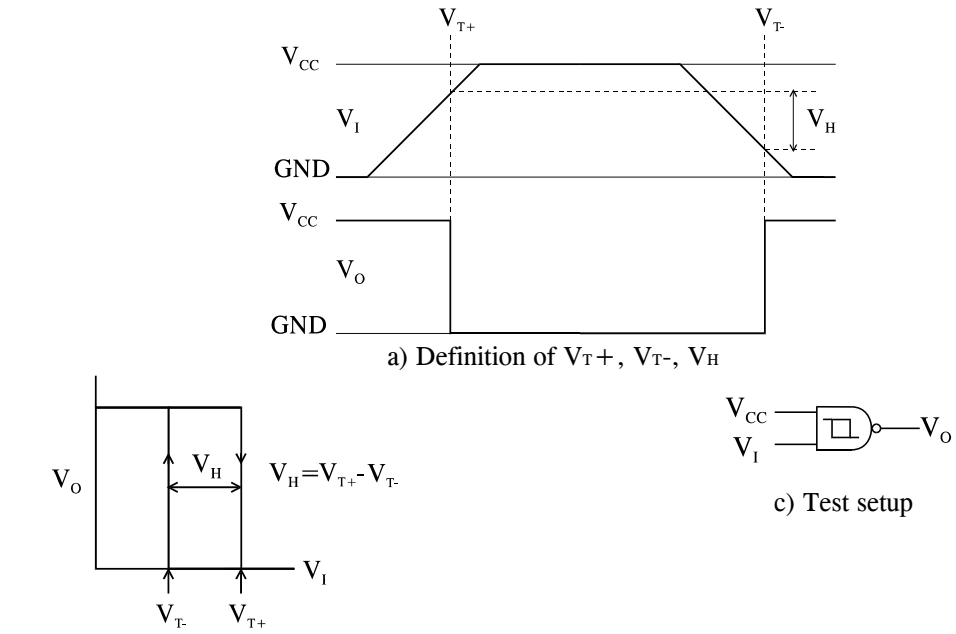


Figure 1. Hysteresis definition, characteristic, and test setup

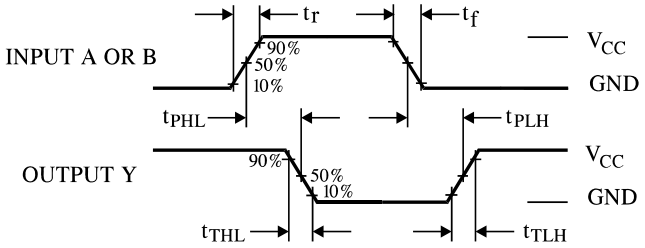
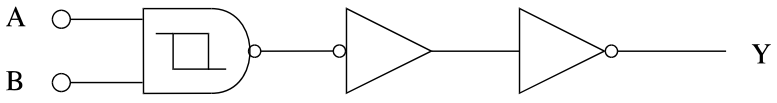
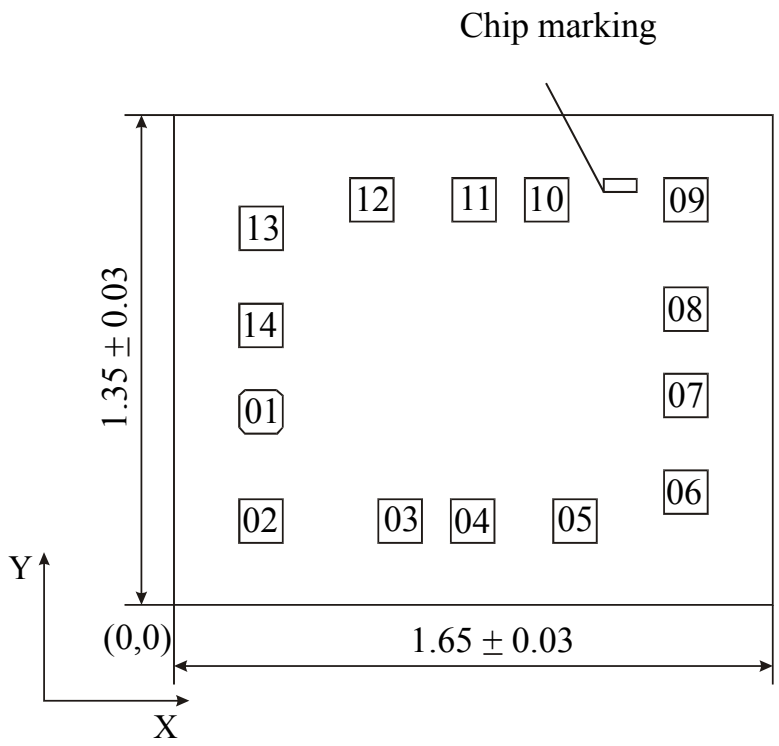


Figure 2. Switching Waveforms

EXPANDED LOGIC DIAGRAM
(1/4 of the Device)



CHIP PAD DIAGRAM



Chip marking :409315
Location of marking (mm): left lower corner x = 1.184, y = 1.138
Chip thickness: 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	A1	0.180	0.472	0.120×0.120
02	B1	0.180	0.171	0.120×0.120
03	Y1	0.563	0.171	0.120×0.120
04	Y2	0.763	0.171	0.120×0.120
05	A2	1.045	0.171	0.120×0.120
06	B2	1.350	0.251	0.120×0.120
07	GND	1.350	0.517	0.120×0.120
08	A3	1.350	0.755	0.120×0.120
09	B3	1.350	1.056	0.120×0.120
10	Y3	0.967	1.056	0.120×0.120
11	Y4	0.767	1.056	0.120×0.120
12	A4	0.485	1.056	0.120×0.120
13	B4	0.180	0.976	0.120×0.120
14	Vcc	0.180	0.710	0.120×0.120

Note: Location is given as per passivation layer