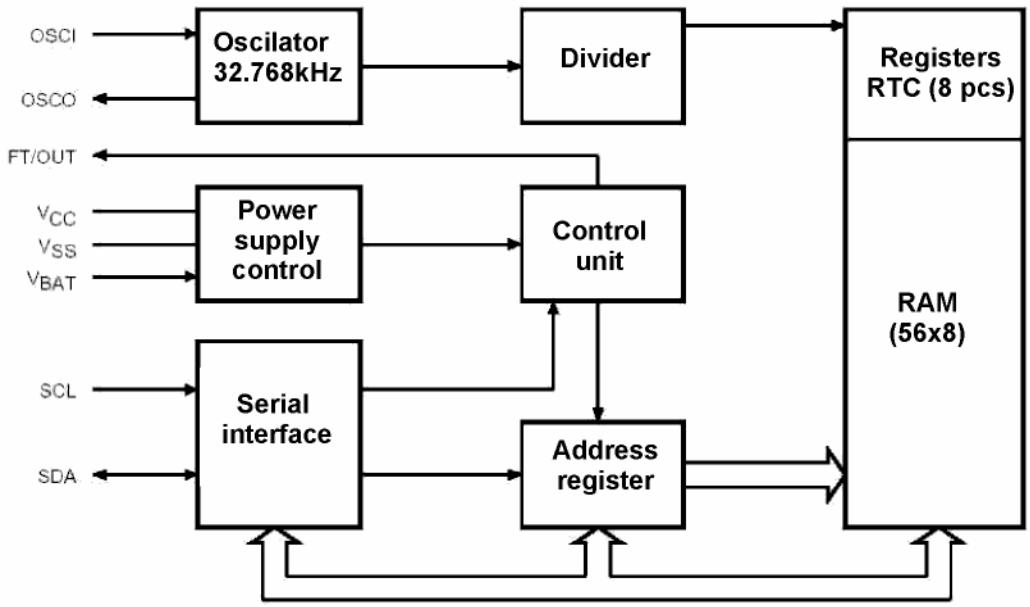
CMOS IC OF REAL TIME WATCH WITH SERIAL INTERFACE

Microcircuit IN1356 is essentially the binary-decimal watch with calendar, has the additional 56 bytes of the nonvolatile static memory and possesses the low power consumption. Addresses and data are transferred in series via the double wire bi-directional bus. The microcircuit is intended for count of the current time in hours, minutes and seconds, count of the week days, date, month and year. The last day of the month is automatically adjusted for the months, fewer, than 31 days, including correction for the leap year. The watch functions in the 24-hour mode. The microcircuit IN1356 has the built-in power supply control circuit, which detects the supply disruption and automatically switches the device to the battery mode. The microcircuit IN1356 has the facility for the run accuracy calibration.

Functions and Features

- Count of seconds, minutes, hours, week days, date, months and years with consideration of the leap years;
- 56 bytes of the nonvolatile memory for the data storage;
- double-wire serial interface;
- automatic supply voltage drop detection and switching diagram;
- consumption of less than 500 nA in the backup supply mode with the operating oscillator;
- operating temperature range: -40°C ÷ +85°C;
- calibration of run accuracy.

Structural Diagram IN1356



IN1356 Operating Temperature Range

Operating temperature range of the microcircuit IN1356: T_A = - 40 ÷ + 85 °C.

Limit Mode IN1356

Limit and limit-permissible operating modes of microcircuit IN1356 are listed in the table:

Parameter Description, Measurement Unit	Identification	Norm			
		Limit Permissible		Limit	
		Not less	Not over	Not less	Not over
Supply voltage, V	V_{CC}	4.5	5.5	-0.3	7.0
Supply voltage from supply element, V	V_{BAT}	2.5	3.5	-0.3	7.0
Low level input voltage, V	V_{IL}	-0.3	1.5	-	-
High level input voltage, V	V_{IH}	3	V_{CC}+0.8	-	-
Signal frequency at input SCL, kHz	f_{SCL}		100	-	-

All voltages are listed relative to the microcircuit common pin. Under influence of the limit mode serviceability of the microcircuits is not guaranteed. After plotting the limit mode serviceability is guaranteed in the limit permissible mode.

IN1356 Electric Parameters

The electric parameters of the IN1356 microcircuit at the temperature T_A = –40 ÷ + 85°C, V_{CC} = 4.5 ÷ 5.5 B are listed in the table

Parameter Description, Measurement Unit	Identification	Measurement Mode	Norm		Type Value	Remark
			Not less	Not over		
Input leakage current, µA	I_{LI}	0V ≤ V_{IN} ≤ V_{CC}	-	1		
Output leakage current, µA	I_{LO}	0V ≤ V_{OUT} ≤ V_{CC}	-	1		
Dynamic consumption current, µA	I_{CC1}	F_{SCL} =100 kHz	-	300		1
Static consumption current, µA	I_{CC2}				100	
Low level output voltage, V	V_{OL}	V_{CC} = 4.5V, I_{OL} = 5mA		0.4		
Consumption current from supply element, nA	I_{BAT}	T_A = 25°C, V_{CC}=0V, Oscillator on., V_{BAT} = 3V		550		2

Remarks:

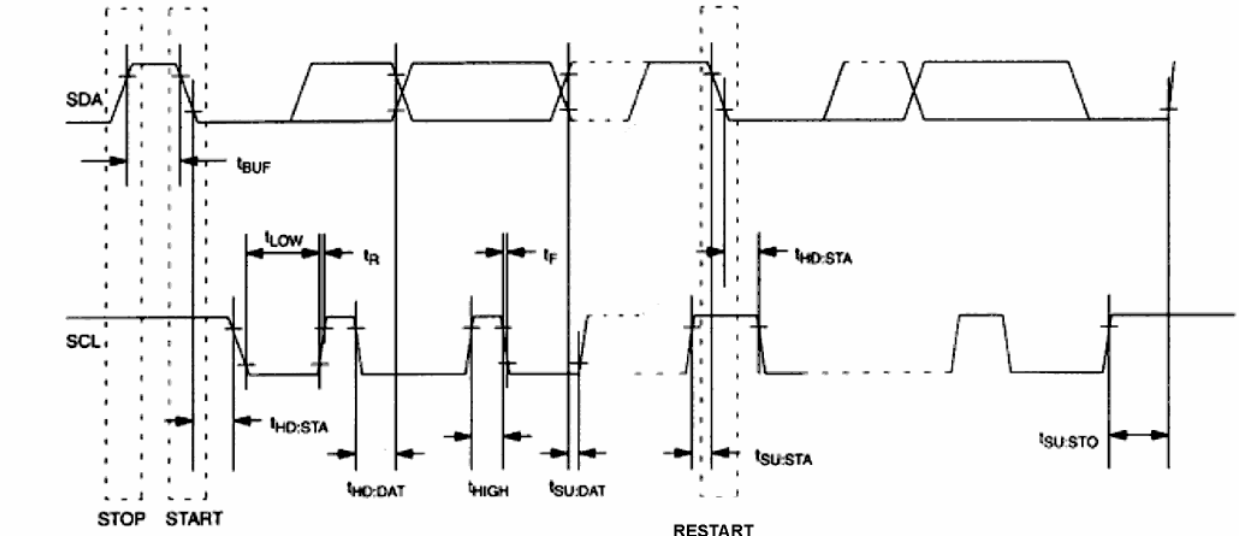
1. Load capacitance at pin SDA - not over 100 pF
2. Parameters of the quartz resonator: f_O = 32.768 kHz, R_S ≤ 60 kOhm, C_L =12.5 pF

Dynamic parameters at the temperature T_A = –40 ÷ +85°C, V_{CC} = 4.5 ÷5.5 B are listed in the table

Parameter Description, Measurement Unit	Identification	Measurement Mode	Norm	
			Not less	Not over
Cycle frequency at input SCL, kHz	f_{SCL}	–	0	100
Vacant bus time between the statuses STOP and START, usec	t_{BUF}	–	4.7	–
Hold time of the status START, usec	$t_{HD:STA}$ 1)	–	4.0	–
Low level duration of the signal SCL, usec	t_{LOW}	–	4.7	–
High level duration of the signal SCL, usec	t_{HIGH}	–	4.0	–
Presetting time for the status START, usec	$t_{SU:STA}$	–	4.7	–
Data presetting time, nsecc	$t_{SU:DAT}$	–	250	–
Data hold time, usec	$t_{HD:DAT}$ 2)	–	0	–
Front duration of the signals SDA and SCL, nsec	t_R	–	–	1000
Drop duration of the signals SDA and SCL, nsec	t_F	–	–	300
Presetting time for the status STOP, usec	$t_{SU:STO}$	–	4.7	–
Total capacitance load on each bus line, pF	C_B	–	–	400
Input or output capacitance, pF	$C_{I/O}$	–	10	10
Load capacitance of the quartz oscillator, pF	C_{LX}	–	12.5	12.5

1) After this time interval the first cycle signal is formed;
2) Device should internally ensure the hold time of the signal SDA of not less, than 300 nsec relative to the high level of the signal SCL in order to overlap the indeterminancy area of the signal SCL drop front.
The maximum value of $t_{HD:DAT}$ should be determined in that case, if the device does not increase duration of the low level (t_{LOW}) of the signal SCL.

Time Parameters Chart



IN1356 Functioning

IN1356 operates as the «slave» device on the serial bus. For access to it it is required to preset the status START and to transfer the register address following the device identification code. To the following registers it is possible to automatically address in series prior to presetting the status STOP. When V_{CC} drops below 1.25 x V_{BAT}, access termination occurs to the device, and the address counter is reset. At this time the device does not recognize the input data, excluding the erroneous information writing. When V_{CC} drops below V_{BAT}, the device switches over to the battery mode, consuming the low current. With power supply V_{CC} above V_{BAT} + 0.2 V the device triggers over from the battery power supply on V_{CC}, and recognizes the input data with V_{CC} above 1.25 x V_{BAT}.

Description of Signals

V_{CC}, V_{SS} – connection of constant supply. V_{CC} – input +5 V. With power supply of 5 V within the normal limits the device is completely accessible for reading and writing the information. When V_{CC} drops below 1.25 x V_{BAT} the 3 -volt supply element is connected to the device, and reading and writing of data is prohibited. However, the time count proceeds, supported by the low supply voltage. When V_{CC} drops below V_{BAT}, then ROM and the time count circuit triggers over to the external power supply source (3 V) V_{BAT}.

V_{BAT} – input for any standard 3-volt lithium supply element or other energy source. For the correct circuit operation the supply element voltage should be within the limits of 2.5 – 3.5 volts. Protection voltage from writing, at which access is terminated to the real time watch and ROM, is set by means of the internal circuit to the value of 1.25 x V_{BAT}. The lithium battery supply source with capacitance of 48 mAhr will support IN1356 in the backup mode (supply voltage **V_{CC}** is unavailable) over 10 years at the temperature 25 °C.

SCL (Synchrosignal input) – SCL is used for synchronization of the data transfer by the serial interface.

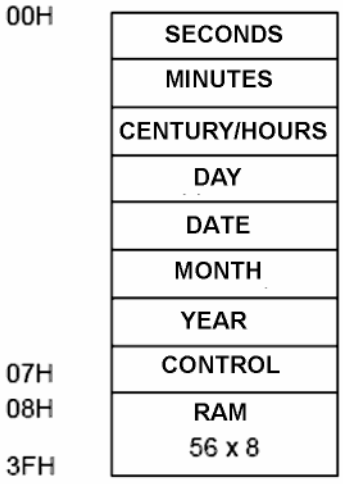
SDA (Input/Output of the serial data) – SDA is the data input/output of the double wire serial interface. The pin SDA is essentially the open drain, for which it is required to have connection of the external load resistor.

FT/OUT (Output of programmed signal) – If the bit FT (frequency test) of the control register is in the high level status, then the output FT/OUT generates the meander with the frequency of 512 Hz. If the bit FT is in the low level status, then the output FT/OUT generates the status (high or low level) of the bit OUT of the control register. Output FT/OUT is essentially the open drain, for which it is required to have connection of the external load resistor. FT/OUT is accessible at V_{CC} and V_{BAT}.

OSCI, OSCO – connection of the standard quartz resonator for the frequency of 32.768 kHz. The capacitance load of the internal oscillator for the quartz resonator is equal to 12 pF. IN1356 can operate from the external oscillator with the frequency of 32.768 kHz. With this configuration the pin OSCI is connected to the external signal oscillator, and OSCO is left disconnected.

Card of Addresses RTC and ROM

Addresses card of the registers RTC (real time clock) and ROM is depicted in the Figure. Registers of the real time watch has the addresses 00H – 07H. ROM registers have the addresses 08H – 3FH. In the mode of the multibyte access the address 3FH (the end of the ROM address space) passes over to the address 00H (end of the address space of the registers RTC).



Watch and Calendar

Acquisition of information about the time and date is performed by means of reading the appropriate register bytes. Registers of the real time watch are indicated in the figure. When turning the power supply on the initial status of all registers is not determined. Presetting and initialization of time and calendar is performed by means of writing the appropriate bytes. Information, contained in the registers of time and calendar, represents itself the binary-decimal code.

The bit ST (stop bit) of the seconds register (address 0) is the bit of the watch stop. When it is set to the high level, then the oscillator is turned off.

Bit CEB (century enable bit) controls the bit status CB (century bit) of the watch register (address 2). If the bit CEB is preset to the high level, then switching of the bit CB occurs from the high level to the low level or from the low level to the high level (it is determined by the initial status) each 100 years. if the bit CEB is preset to the low level, then switching of the bit CB is blocked, and it is in the initial status.

IN1356 operates in the 24-hour mode.

With the next emergence of the status START at the input SDA writing occurs of the current time from the counters to the appropriate registers (with the primary emergence of the status START relative to supply activation of the microcircuit writing of the current time is unavailable). The data about time from these registers are read in series byte by byte by means of indicating their addresses, and the watch continues to operate.

Registers RTC IN1356

Address	Data								Registers / Range	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST	Tens of seconds			Units of seconds				Seconds	00 – 59
1	X	Tens of minutes			Units of minutes				Minutes	00 – 59
2	CEB	CB	Tens of hours		Units of hours				Century / Hours	0-1/ 00 – 23
3	x	x	x	x	x	Day of week			Day of week	01 – 07
4	x	x	Tens of date		Units of date				Dates	01 – 31
5	x	x	x	10 M.	Units of month				Month	01-12
6	Tens of years				Units of years				Year	00 – 99
7	OUT	FT	S						Control	

Control Register

Control register (address 7) is used for control of the pin FT/OUT and alignment of the watch run. If the bit FT (frequency test) is in the high level status, then the pin FT/OUT generates the meander with the frequency of 512 Hz. If the bit FT is in the low level status, then the output FT/OUT generates the status (high level or low level) of the bit OUT. The bit S (sign bit) and five junior digits of the control register preset the frequency calibration value.

Real time watch run accuracy depends on the quartz resonator and the temperature drift of its characteristics. In order to ensure the requirements of some systems the microcircuit contains the module of the digital run alignment, which ensures the time correction up to +126.108 ppm or -63.054 ppm (ppm – parts per million or a million part). The alignment value is preset by the operand in the control register: 5 junior register digits preset the alignment value and can assume the value 0 ÷ 31, and the 6-th digit determines the alignment sign (positive or negative). If the value of 5 junior register digits is equal to 0, then alignment is not in effect. Operand in the register is represented in the binary format.

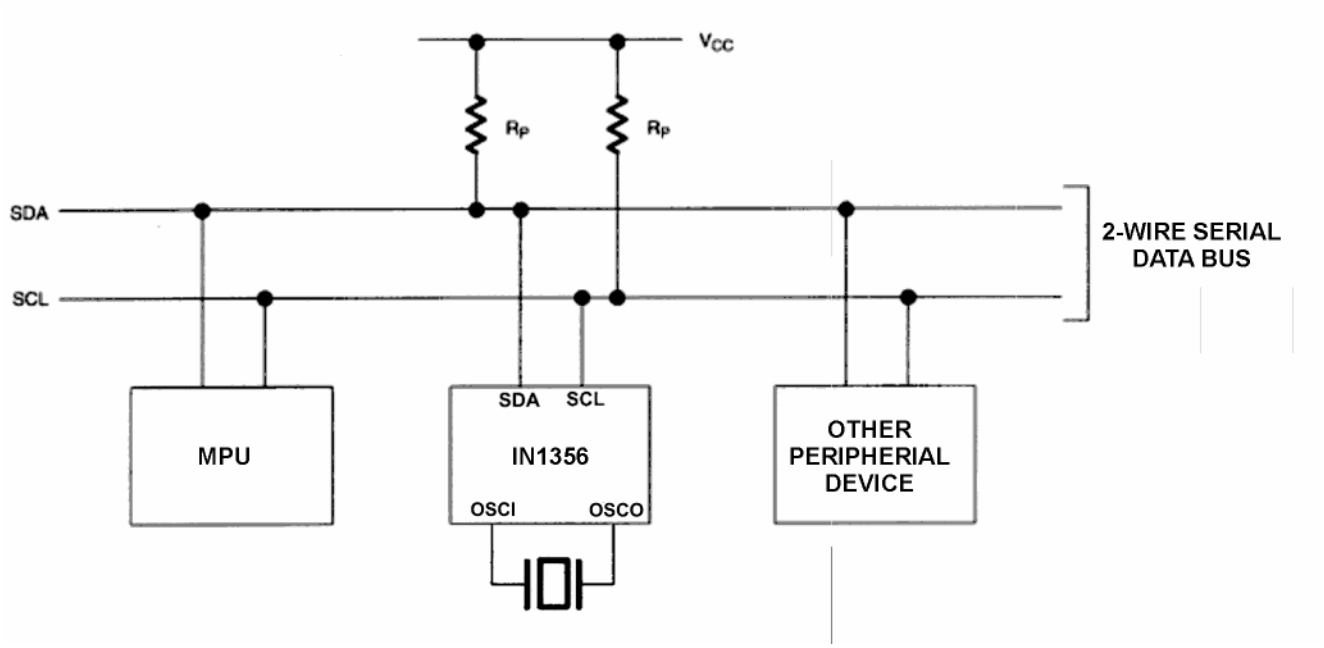
Calibration

The system analyzes the 512 Hz frequency at the output FT/OUT of the microcircuit and then loads the appropriate alignment operand into the control register. The 512 Hz frequency reflects the frequency deviation of the quartz resonator frequency. Alignment is performed inside the 64 minute cycle within the first 62 minute cycles, in each of them only one second is corrected by means of replacement of one 128 Hz pulse by two 256 Hz pulses in case of the positive alignment (second is shortened) or exclusion of one 256 Hz pulse in case of the negative alignment (second is prolonged). Such mechanism ensures the alignment accuracy in the 64 minute cycle: with the positive alignment the accuracy is equal to + 2.034 ppm ((256 cycles/(32768 cycles x 60 seconds x 64 minutes)) x 1000000 = 2.034); with the negative alignment the accuracy is equal to – 1.017 ppm ((128 cycles/(32768 cycles x 60 seconds x 64 minutes)) x 1000000 = 1.017). If the correction operand value in the control register is equal to 1, then the first 2 minutes in the 64 minute cycle will be corrected and the accuracy of one correction step is equal to 4.068 ppm (2.034 x 2 = 4.068) or – 2.034 ppm (1.017 x

2 = 2.034), if the correction operand value is equal to 6, then the first 12 minutes will be corrected in the 64 minute cycle and the correction accuracy will be equal to + 24.408 ppm or – 12.204 ppm and etc.

Double Wire Serial Data Bus

IN1356 supports the bi-directional double wire bus and its data transfer protocol. The bus can be controlled by the "master" device, which generates the cycle signal (SCL), controls access to the bus, generates the statuses START and STOP. The typical bus configuration with the double wire protocol is indicated in the Figure.



Data transfer can be start only when the bus is not busy. In the process of the data transfer the data line should remain stable, while the cycle signal line is in the high level status. Alterations of the data line status at that moment, when the cycle line is in the high status, will be understood as the control signals.

In compliance with this the following conditions are determined:

Bus is not busy: both lines of data and cycle signal are in the HIGH status.

Beginning of data transfer: alteration of the data line status with transition from HIGH to LOW, while the cycle line is in the HIGH status, is determined as the status START.

Data transmission stop: Alteration of the data line status with transition from LOW to HIGH, while the cycle line is in the HIGH status, is determined as the status STOP.

Informational data: Data line status complies with the informational data, when after the status START the data line is stable at the time of the HIGH status of the cycle signal. The data on the line should be altered at the time of the LOW status of the cycle signal. One cycle pulse per one data bit.

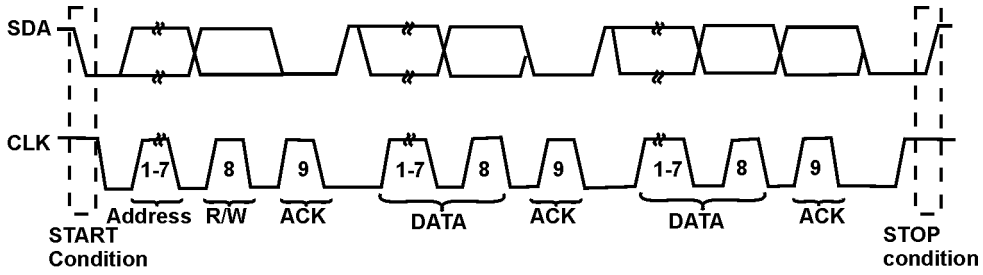
Each data transfer starts vwith arrival of the status START and stops with arrival of the status STOP. Number of data bytes, transferred between the statuses START and STOP, is not limited and deter-

mined by the «master» device. Information is transferred byte by byte, and each byte receipt is confirmed by the ninth bit. The data transfer is performed at the frequency of 100 kHz.

Reception confirmation: Each receiving device after reception of each byte generates the receipt confirmation bit.. The «master» device should generate the additional cycle pulses, which are set in compliance with the confirmation bits.

If the receipt confirmation signal is in the high status, then upon arrival of the cycle pulse confirmation, confirming receipt, the device should switch the line SDA in the low status. Of course, one should take into consideration the presetting time and the hold time. The «master» device should signalize about the data transfer completion to the «slave» device, stopping the confirmation bit generation, upon receipt from the «slave» cycle pulse of the reception confirmation. In this case, the «slave» one should switch the data line to the low status, in order to make it possible for the «master» one to generate the status STOP.

Data transfer by the serial double wire bus



Depending on the status of the bit $R/\overline{W}$, two types of transmission are possible:

1.**The data are transferred from the «master» transmitter to the «slave» receiver.** The first byte, transmitted by the «master» one, is the address of the «slave» one. Then follows the data bytes sequence. The «slave» one returns the reception confirmation bits after each received byte. Data transmission order: the first one is the senior most digit (MSB).

2.**Data are transferred from the «slave» transmitter to the «master» receiver.** The first byte (address of the «slave» one) is transferred to the «master» one. Then the «master» one returns the confirmation bit. This follows after transmission by the «slave» one of the data sequence. The «master» returns the reception confirmation bit after each received byte with exception of the last byte. After reception of the of the last byte the reception confirmation bit is not returned.

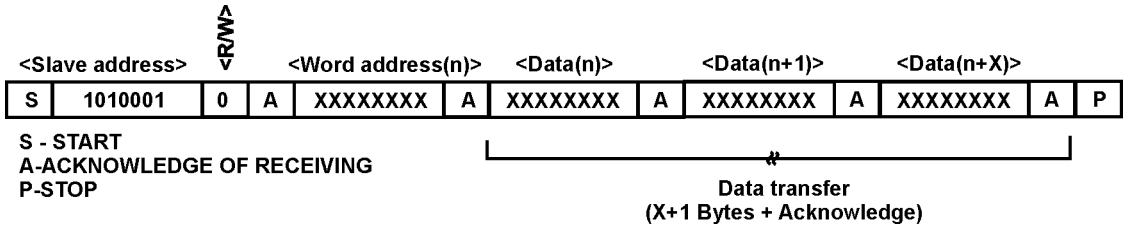
The «master» device generates all cycle pulses and statuses START and STOP. Transmission is completed after emergence of the status STOP or the repeated emergence of the status START. As the repeated status START is the beginning of the next serial transmission, the bus is not vacated. The data transmission order: the first one is the senior most digit (MSB).

IN1356 can operate in the two following modes:

1. **Mode of the «slave» receiver (writing mode IN1356):** The serial data and cycles are received via SDA and SCL appropriately. After transmission of each byte the confirming bit is transmitted. The

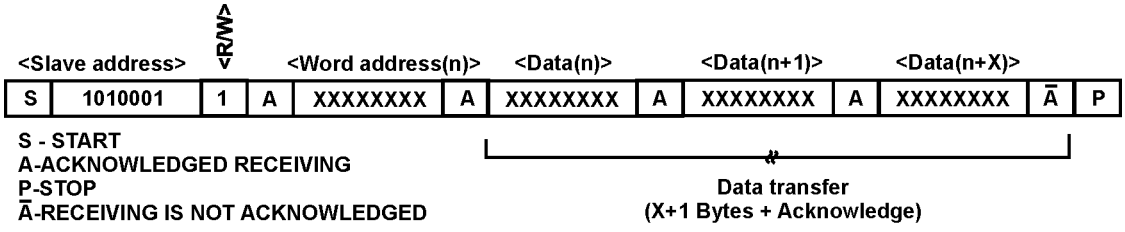
statuses START and STOP are considered as the start and end of the serial transmission. The address identification is performed by the hardware means after the address reception of the «slave» one and the direction bit. The address byte is the first byte, received after emergence of the status START, generated by the «master» one. The address byte is equal to 1101000 (seven senior bits) of the address and is accompanied by the transfer direction bit ($R/\overline{W}$) (junior digit), which is equal to 0 for writing. After reception and decoding the address byte IN1356 will generate confirmation on the line SDA. After confirmation by IN1356 of the «slave» one address and the writing bit, the «master» one will transfer the register address of IN1356. Thus, the register indicator of IN1356 will be preset. Then the «master» one will transfer each data byte with the serial reception of each byte receipt confirmation. Upon completion of writing the «master» will form the status STOP, for termination of the data transfer.

Data Writing – Mode of «Slave» Receiver



2. **Mode of «slave» transmitter (mode of writing from IN1356):** The first byte is received and processed as in the mode of the «slave» receiver. However, in this mode the direction bit will show, that the transfer direction is altered. The serial data are transferred by IN1356 on SDA, the cycle pulses - on SCL. The statuses START and STOP are identified as the start and end of the serial transmission. The address byte is the first byte, received after emergence of the status START, generated by the «master» one. The address byte is equal to 1101000 (seven senior bits) address and is accompanied by the transfer direction bit ($R/\overline{W}$) (junior digit), which is equal to 1 for reading. After reception and the address byte decoding IN1356 accepts confirmation from the line SDA. Then IN1356 starts to transmit the data from the address, to which shows the register indicator. If the register indicator is not written prior to initialization of the read-out mode, then the first read address is the last address, stored in the register indicator. IN1307 should send the «non-confirmation» bit, in order to complete reading.

Data Reading – Mode of «Slave» Receiver



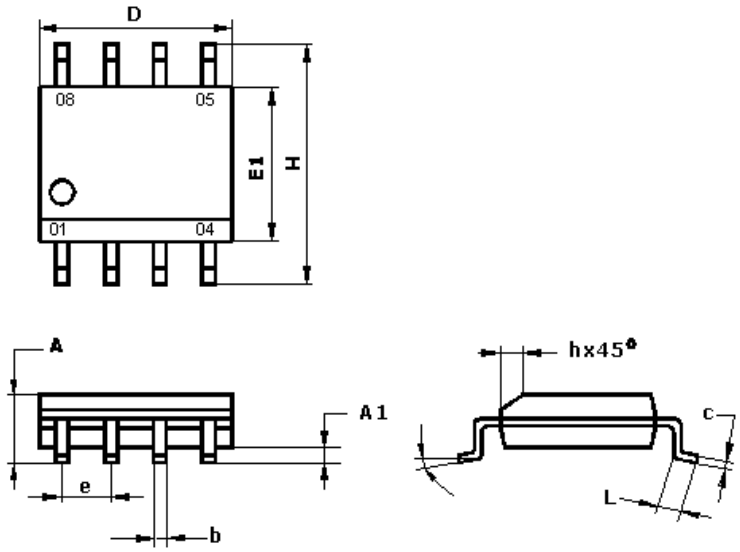
Note: last byte is followed by bit receiving is not acknowledged

Purpose of IN1356 Pins

Pin Number	Identification	Purpose
01	OSCI	Input for connection of the quartz resonator
02	OSCO	Output for connection of the quartz resonator
03	V_{BAT}	Supply pin from the battery voltage source
04	V_{SS}	Common pin
05	SDA	Input-output of the serial data
06	SCL	Input of synchrosignal
07	FT/OUT	Output of programmed signal
08	V_{CC}	Supply pin from voltage source

Package Dimensional Sizes

SOP8 150 mil (MS-012AA)



	D	E1	H	b	e	α	A	A1	c	L	h
Millimeters											
min	4.80	3.80	5.80	0.33		0°	1.35	0.10	0.19	0.41	0.25
max	5.00	4.00	6.20	0.51	1.27	8°	1.75	0.25	0.25	1.27	0.50
Inches											
min	0.1890	0.1497	0.2284	0.013		0°	0.0532	0.0040	0.0075	0.016	0.0099
max	0.1968	0.1574	0.2440	0.020	0.100	8°	0.0688	0.0090	0.0098	0.050	0.0196