IN74LV573

Octal D-type transparent latch (3-State)

The 74LV573 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT573.

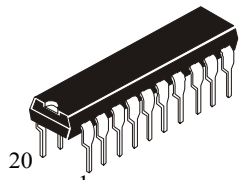
The 74LV573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable (OE) input are common to all internal latches.

The '573' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When OE is LOW, the contents of the eight latches are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of the latches.

The '573' is functionally identical to the '563' and the '373', but the '563' has inverted outputs and the '373' has a different pin arrangement.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL IC_S
- Supply voltage range: 1.0 to 5.5 V
- Low input current: 1.0 μA; 0.1 μA at T = 25 °C
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX
PLASTIC DIP

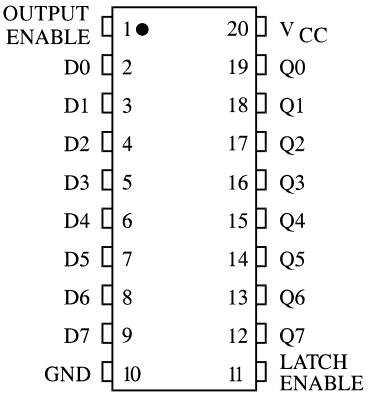
DW SUFFIX
SO

ORDERING INFORMATION

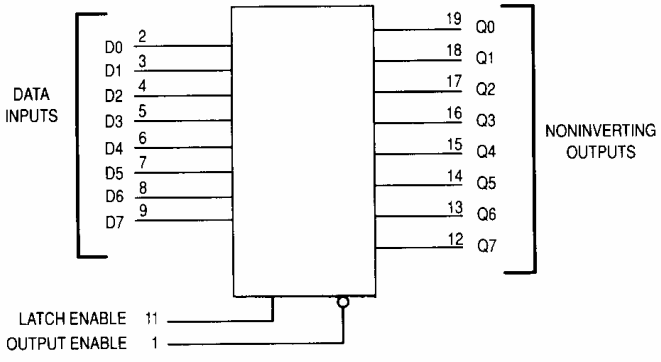
IN74LV573N	Plastic DIP
IN74LV573DW	SOIC
IZ74LV573	chip

T_A = -40° to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

FUNCTION TABLE

Inputs			Output
Output Enable	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L,H, ↓	X	no change
H	X	X	Z

H= high level
L = low level
X = don't care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +7.0	V
I_{IK} *1	Input diode current	±20	mA
I_{OK} *2	Output diode current	±50	mA
I_O *3	Output source or sink current	±35	mA
I_{CC}	V_{CC} current	±70	mA
I_{GND}	GND current	±50	mA
P_D	Power dissipation per package: Plastic DIP *4 SO *4	 750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*1 $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V.
*2 $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V.
*3 -0.5 V $< V_O < V_{CC} + 0.5$ V.
*4 Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SO Package: - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.2	5.5	V
V_I	DC Input Voltage		0	V_{CC}	V
V_O	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0 V ≤ V_{CC} ≤ 2.0 V 2.0 V ≤ V_{CC} ≤ 2.7 V 2.7 V ≤ V_{CC} ≤ 3.6 V 3.6 V ≤ V_{CC} ≤ 5.5 V	0 0 0 0	500 200 100 50	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parame-ter	Test conditions	V_{CC} V	Guaranteed Limit								Unit
				25°C		-40°C		85°C		125°C		
				min	max	min	max	min	max	min	max	
V_{IH}	HIGH level input voltage		1.2 2.0 2.7 3.0 3.6 4.5 5.5	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	V
V_{IL}	LOW level output voltage		1.2 2.0 2.7 3.0 3.6 4.5 5.5	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	V
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = -100 μA	1.2 2.0 2.7 3.0 3.6 4.5 5.5	1.05 1.85 2.55 2.85 3.45 4.35 5.35	- - - - - - -	1.05 1.85 2.55 2.85 3.45 4.35 5.35	- - - - - - -	1.0 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	1.0 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	V
		$V_I = V_{IH}$ or V_{IL} I_O = -8 mA	3.0	2.48	-	2.48	-	2.40	-	2.20	-	V
		$V_I = V_{IH}$ or V_{IL} I_O = -16 mA	4.5	3.70	-	3.70	-	3.60	-	3.50	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = 100 μA	1.2 2.0 2.7 3.0 3.6 4.5 5.5	- - - - - - -	0.15 0.15 0.15 0.15 0.15 0.15 0.15	- - - - - - -	0.15 0.15 0.15 0.15 0.15 0.15 0.15	- - - - - - -	0.2 0.2 0.2 0.2 0.2 0.2 0.2	- - - - - - -	0.2 0.2 0.2 0.2 0.2 0.2 0.2	V
		$V_I = V_{IH}$ or V_{IL} I_O = 8 mA	3.0	-	0.33	-	0.33	-	0.40	-	0.50	V
		$V_I = V_{IH}$ or V_{IL} I_O = 16 mA	4.5	-	0.40	-	0.40	-	0.55	-	0.65	V
I_I	Input current	$V_I = V_{CC}$ or 0 V	5.5	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0 V I_O = 0 μA	5.5	-	8.0	-	8.0	-	80	-	160	μA
I_{CC1}	Additional supply current per input	$V_I = V_{CC}$ – 0.6V	2.7 3.6	-	0.2	-	0.2	-	0.5		0.85	mA
I_{OZ}	Three state leakage current	3-state output V_I (11) = V_{IH} $V_O = V_{CC}$ or 0 V	5.5	-	±0.5	-	±0.5	-	±5	-	±10	μA

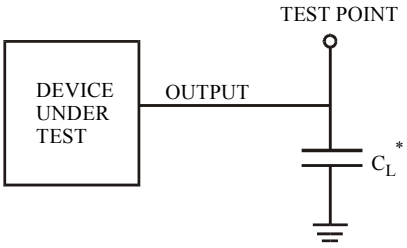
AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, t_r=t_f=2.5 ns)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH}	Propagation delay , Clock to Q	V_I = 0 V or V_I Figures 1,3	1.2	-	150	-	160	-	170	ns
			2.0	-	30	-	39	-	49	
			2.7	-	23	-	29	-	36	
			3.0	-	18	-	23	-	29	
			4.5	-	15	-	19	-	24	
t_{PHL}, t_{PLH}	Propagation delay , LE to Q	V_I = 0 V or V_I Figures 1,3	1.2	-	160	-	180	-	190	ns
			2.0	-	34	-	43	-	53	
			2.7	-	28	-	31	-	34	
			3.0	-	20	-	25	-	31	
			4.5	-	17	-	21	-	26	
t_{PHZ}, t_{PLZ}	Propagation delay, OE to Q	V_I = 0 V or V_I Figures 2,4	1.2	-	160	-	160	-	170	ns
			2.0	-	31	-	39	-	48	
			2.7	-	23	-	29	-	36	
			3.0	-	20	-	24	-	29	
			4.5	-	17	-	20	-	24	
t_{PZH}, t_{PZL}	Propagation delay, OE to Q	V_I = 0 V or V_I Figures 2,4	1.2	-	140	-	160	-	170	ns
			2.0	-	28	-	37	-	48	
			2.7	-	22	-	28	-	35	
			3.0	-	17	-	22	-	28	
			4.5	-	14	-	18	-	23	
C_I	Input capacitance		5.0	-	7.0*	-	-	-	-	pF
C_{PD}	Power dissipation capacitance (per latch)	V_I = 0 V or V_{CC}	5.5	-	52*	-	-	-	-	pF

* T = 25°C

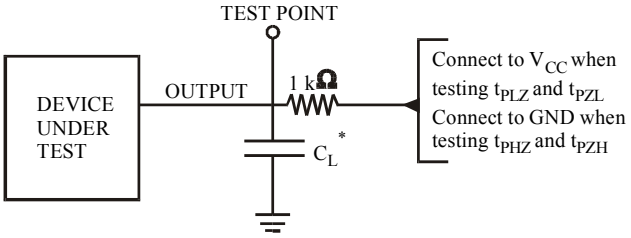
TIMING REQUIREMENTS (C_L=50 pF, t_r=t_f=2.5 ns)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
t_w	Pulse Width, LE (low or high)	V_I = 0 V or V_I Figures 1,3	1.2	100	-	125		150		ns
			2.0	29	-	34	-	41	-	
			2.7	21	-	25	-	30	-	
			3.0	17	-	20	-	24	-	
			4.5	15	-	18	-	21	-	
t_{su}	Setup Time, Data to LE	V_I = 0 V or V_I Figures 1,5	1.2	50	-	75		100		ns
			2.0	15	-	17	-	20	-	
			2.7	11	-	13	-	15	-	
			3.0	8	-	10	-	12	-	
			4.5	6	-	8		10		
t_h	Hold Time, LE to Data	V_I = 0 V or V_I Figures 1,5	1.2	40	-	40	-	40	-	ns
			2.0	8	-	8	-	8	-	
			2.7	8	-	8	-	8	-	
			3.0	8	-	8	-	8	-	
			4.5	8	-	8	-	8	-	



* Includes all probe and jig capacitance

Figure 1. Test Circuit



* Includes all probe and jig capacitance

Figure 2. Test Circuit

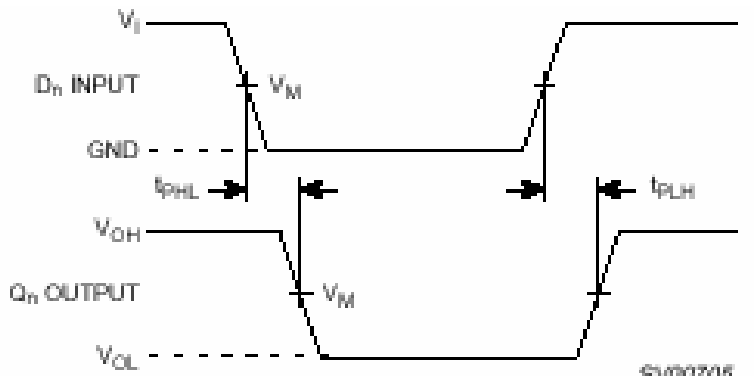


Figure 3. Switching Waveforms

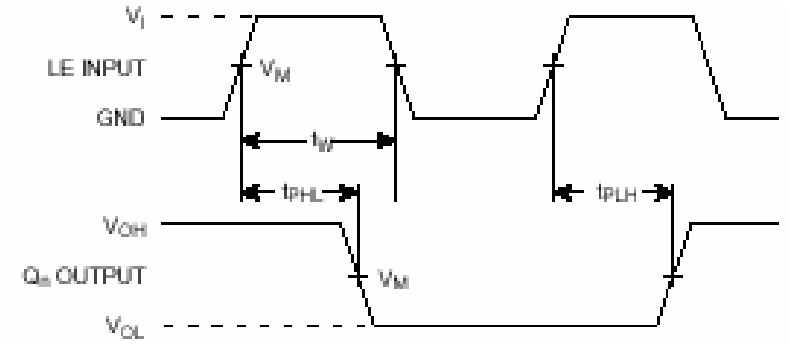


Figure 4. Switching Waveforms

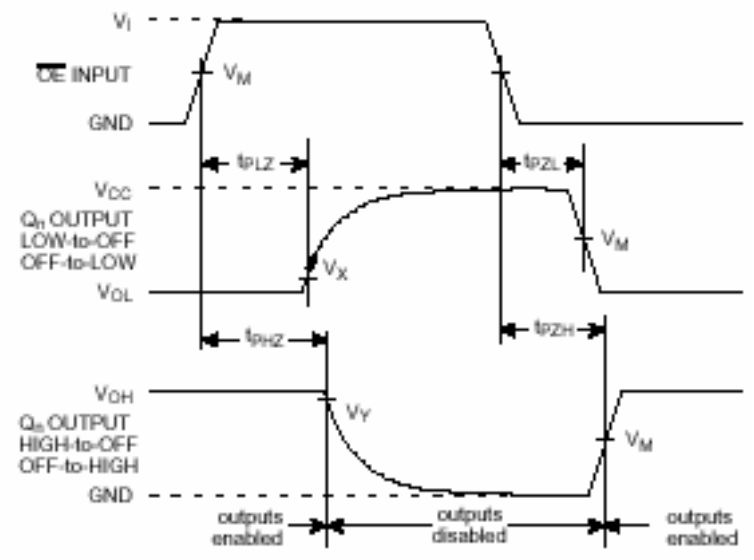


Figure 5. Switching Waveforms

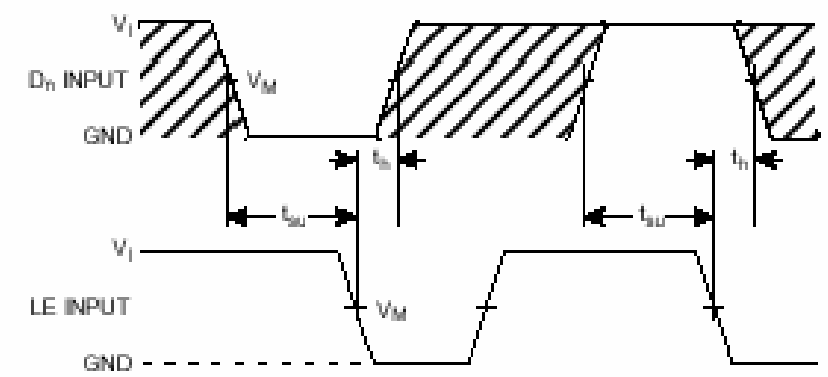
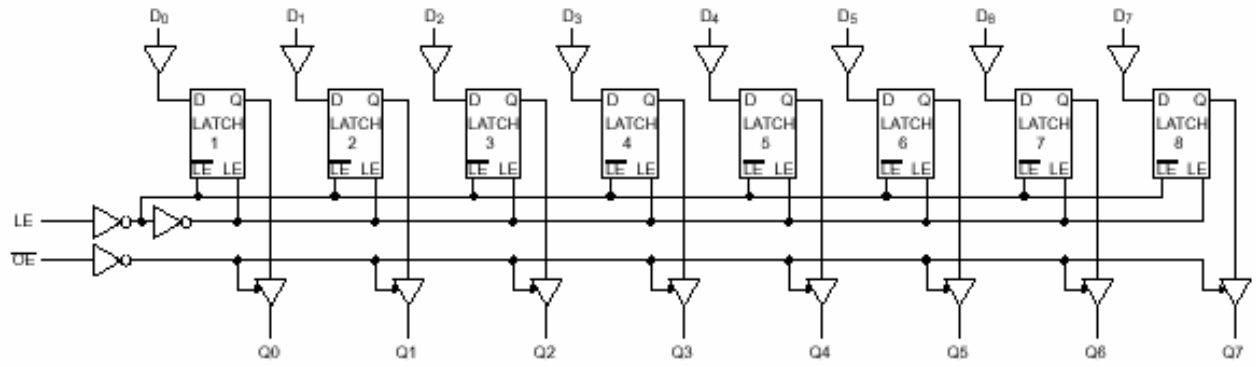


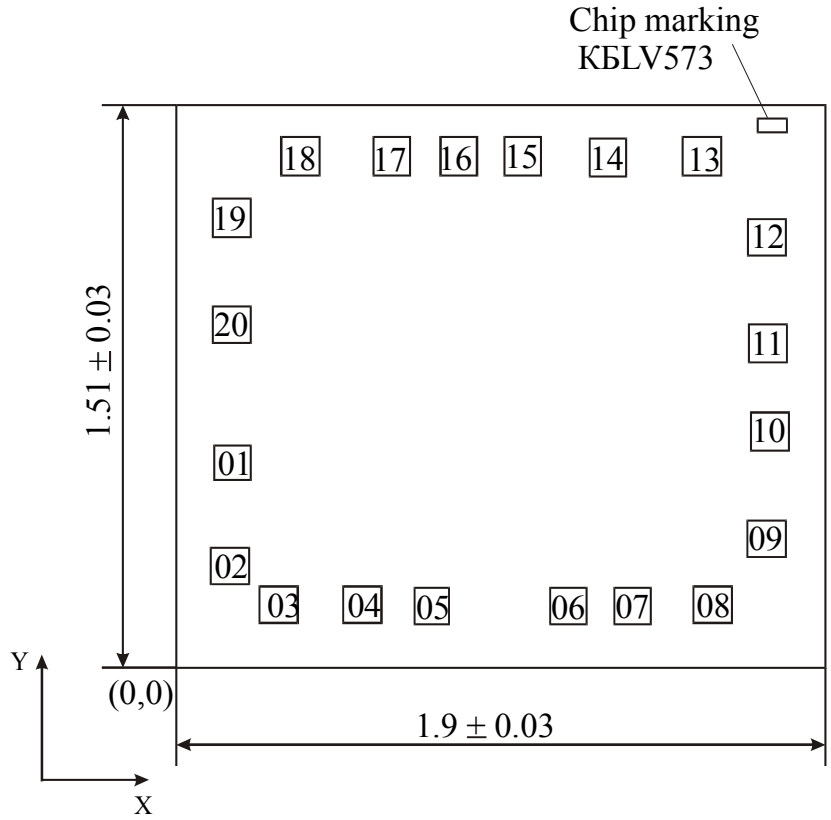
Figure 6. Switching Waveforms

Symbol	V_{CC}, V	Temperature, °C		
		-40°C to 25	85	125
		Level of a signal		
		V	V	V
V_I	1.2	1.2	1.2	1.2
	2.0	2.0	2.0	2.0
	2.7	2.7	2.7	2.7
	3.0	2.7	2.7	2.7
	4.5	4.5	4.5	4.5
V_M	1.2	0.6	0.6	0.6
	2.0	1.0	1.0	1.0
	2.7	1.5	1.5	1.5
	3.0	1.5	1.5	1.5
	4.5	2.25	2.25	2.25
V_X	1.2	0.32	0.37	0.37
	2.0	0.4	0.45	0.45
	2.7	0.55	0.6	0.65
	3.0	0.6	0.65	0.7
	4.5	0.85	0.90	1.0
V_Y	1.2	0.88	0.78	0.68
	2.0	1.5	1.4	1.3
	2.7	2.1	2.0	1.9
	3.0	2.3	2.2	2.1
	4.5	3.45	3.35	3.25

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x=1.656, y=1.353.
Chip thickness: 0.46 ± 0.02 mm, (0.35 ± 0.02 mm – for SOIC).

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	Output enable	0.128	0.545	0.108 x 0.108
02	D 0	0.128	0.229	0.108 x 0.108
03	D 1	0.330	0.120	0.108 x 0.108
04	D 2	0.576	0.120	0.108 x 0.108
05	D 3	0.738	0.120	0.108 x 0.108
06	D 4	1.054	0.120	0.108 x 0.108
07	D 5	1.216	0.120	0.108 x 0.108
08	D 6	1.466	0.120	0.108 x 0.108
09	D 7	1.682	0.314	0.108 x 0.108
10	GND	1.682	0.533	0.108 x 0.108
11	Clock	1.682	0.839	0.108 x 0.108
12	Q 7	1.682	1.108	0.108 x 0.108
13	Q 6	1.422	1.274	0.108 x 0.108
14	Q 5	1.149	1.274	0.108 x 0.108
15	Q 4	0.971	1.274	0.108 x 0.108
16	Q 3	0.811	1.274	0.108 x 0.108
17	Q 2	0.633	1.274	0.108 x 0.108
18	Q 1	0.360	1.274	0.108 x 0.108
19	Q 0	0.128	1.108	0.108 x 0.108
20	V_{CC}	0.128	0.854	0.108 x 0.108

Note: Pad location is given as per metallization layer