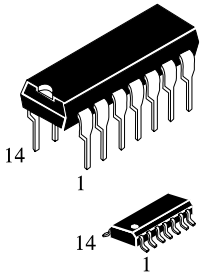
IN74LS07

Hex Non-Inverted Buffers with Open-Collector Outputs



ORDERING INFORMATION

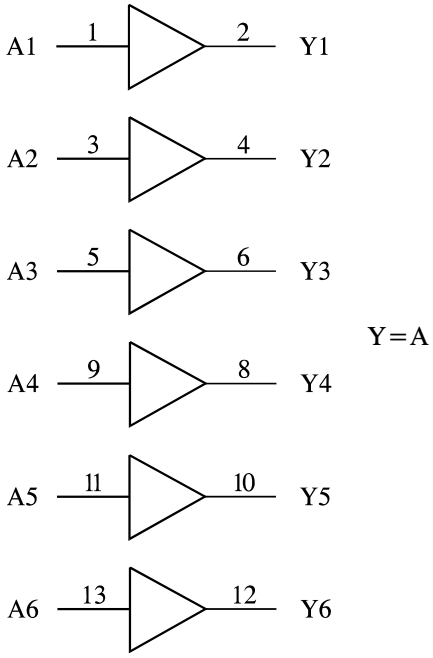
IN74LS07N	Plastic
IN74LS07D	SOIC

T_A = 0° to 70° C for all packages

This device contains hex non inverted buffers with open-collector.

- High Output Voltage 30 V
- High Speed t_{PD} = 12 ns
- Low Power Dissipation P_D = 13 mW per Gate

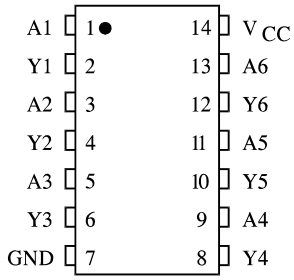
LOGIC DIAGRAM



Y = A

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs	Output
A	Y
H	H
L	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7.0	V
V_{IN}	Input Voltage	5.5	V
V_{OUT}	Output Voltage	30	V
Tstg	Storage Temperature Range	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IH}	High Level Input Voltage	2.0		V
V_{IL}	Low Level Input Voltage		0.8	V
V_{OH}	High Level Output Voltage		30	V
I_{OL}	Low Level Output Current		40	mA
T_A	Ambient Temperature Range	0	+70	°C

DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter	Test Conditions		Guaranteed Limit		Unit
				Min	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.75, I_{IN} = -18 mA			-1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.75, V_{OH}= 5.25			250	µA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75, I_{OL} = 16 mA			0.4	V
		V_{CC} = 4.75, I_{OL} = 40 mA			0.7	
I_{IH}	High Level Input Current	V_{CC} = 5.25, V_{IN} = 2.7 V			20	µA
		V_{CC} = 5.25, V_{IN} = 5.5 V			1	mA
I_{IL}	Low Level Input Current	V_{CC} = 5.25, V_{IN} = 0.4 V			-0.2	mA
I_{CC}	Supply Current	V_{CC} = 5.25	Total with outputs high		14	mA
			Total with outputs low		45	

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF, R_L = 100 Ω,t_r = 15 ns, t_f = 6.0 ns)

Symbol	Parameter	Min	Max	Unit
t_{PLH}	Propagation Delay, Input A to Output Y		10	ns
t_{PHL}	Propagation Delay, Input A to Output Y		30	ns

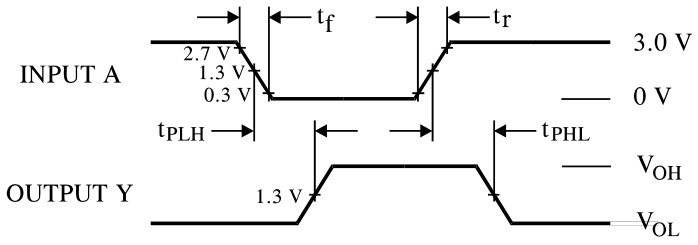
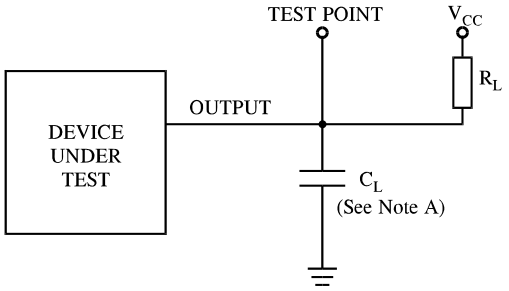


Figure 1. Switching Waveforms



NOTE A. C_L includes probe and jig capacitance.

Figure 2. Test Circuit