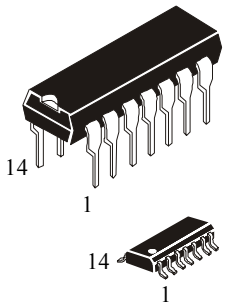
IL324N

Low Power Quad Operational Amplifier

The IL324 contains four independent high gain operational amplifiers with internal frequency compensation. The op-amps operate over a wide voltage range. The device has low power supply current drain, regardless of the power supply voltage. The low power drain makes the IL324 a good choice for battery operation.

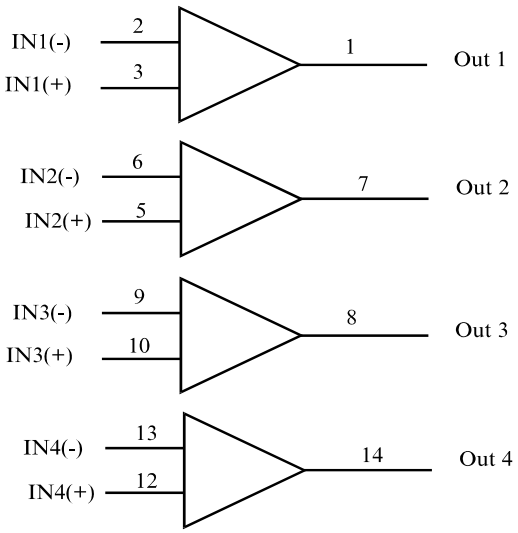
- Internally frequency compensated for unity gain
- Large DC voltage gain
- Single or split supply operation
- Input common-mode voltage range to ground
- Large output voltage swing: 0V DC to V_{CC}-1.5V DC
- Power drain suitable for battery operation
- Low input offset voltage and offset current
- Differential input voltage range equal to the power supply voltage



ORDERING INFORMATION

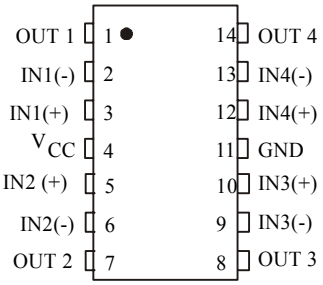
IL324N	Plastic
IL324D	SOIC
IZ324	Chip

BLOCK DIAGRAM



PIN 4 = V_{CC}
PIN 11= GND

PIN ASSIGNMENT



INTEGRAL

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltages Single Supply Split Supplies	 32 ±16	 V
V_{IDR}	Input Differential Voltage Range (1)	±32	V
V_{ICR}	Input Common Mode Voltage Range	-0.3 to 32	V
t_s	Short-Circuit duration of Output	100	ms
T_J	Junction Temperature Plastic Packages	 150	 °C
Tstg	Storage Temperature Plastic Packages	 -55 to +125	°C
I_{IN}	Input Current, per pin (2)	50	mA
T_L	Lead Temperature, 1mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
Notes:
1. Split Power Supplies.
2. V_{IN}<-0.3V.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	±2.5 or 5.0	±15 or 30	V
T_A	Operating Temperature, All Package Types	0	+70	°C

DC ELECTRICAL CHARACTERISTICS (T_A=0 to +70°C)

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V_{IO}	Maximum Input Offset Voltage	V_{CC}=5.0-30V;R_S=0Ω V_O=1.4V V_{ICR}=0V - (V_{CC}-1.5V)* V_{ICR}=0V - (V_{CC}-2.0V)		 7.0* 9.0	mV
I_{IO}	Maximum Input Offset Current	V_{CC}=5.0-30V, V_O =1.4V		±50* ±150	nA
I_{IB}	Maximum Input Bias Current	V_{CC}=5.0-30V, V_O =1.4V		-250* -500	nA
V_{ICR}	Input Common Mode Voltage Range	V_{CC}=30V	0	V_{CC}-1.5V V_{CC}-2.0V	V
I_{CC}	Maximum Power Supply Current	R_L=∞,V_{CC}=5V, V_0=2.5V R_L=∞,V_{CC}=30V, V_0=15V		1.2 3.0	mA
A_{VOL}	Minimum Large Signal Open-Loop Voltage Gain	V_{CC}=15V, R_L≥2KΩ	25* 15		V/mV
V_{OH}	Minimum Output High-Level Voltage Swing	V_{CC}=5V,R_L=2KΩ V_{CC}=30V,R_L=2KΩ V_{CC}=30V,R_L=10KΩ	3.3 26 27		V
V_{OL}	Maximum Output Low-Level Voltage Swing	V_{CC}=5V,R_L=10KΩ		20	mV
CMR	Common Mode Rejection	V_{CC}=5-30V, R_S=10KΩ	65*		dB
PSR	Power Supply Rejection	V_{CC}=5-30V	65*		dB
I_{SC}	Maximum Output Short Circuit to GND	V_{CC}=5.0V, V_O=0V		60*	mA
I_{O+}	Minimum Output Source Current	V_{CC}=15V, V_{ID-}=1.0V,	20*		mA
I_{O-}	Minimum Output Sink Current	V_{ID}=-1.0V, V_{CC}=15V, V_O=15V V_{ID}=-1.0V, V_{CC}=15V, V_O=0.2V	10* 5 12*		mA mA µA
V_{IDR}	Differential Input Voltage Range	All V_{IN}≥GND or V-Supply (if used)		V_{CC}*	V

* T_A = +25°C

NOTE: Guaranteed Limits of DC Electrical Characteristics are given for T_A=0, +70°C as the information for chips.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A= +25ºC)

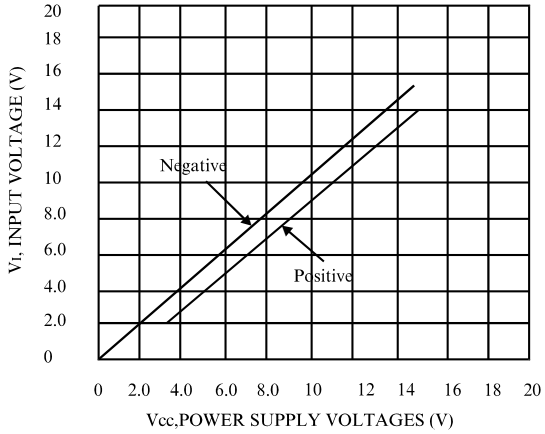


Figure 1.Input Voltage Range

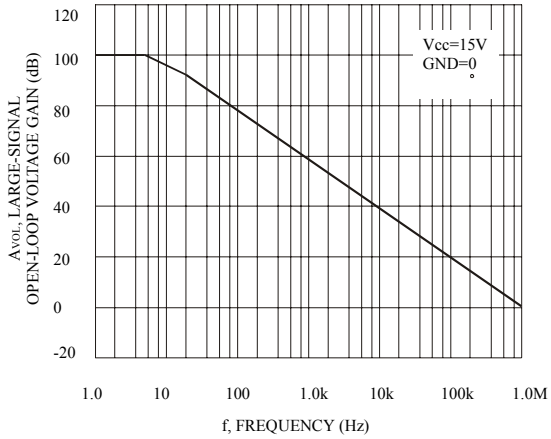


Figure 2. Open-Loop Frequency

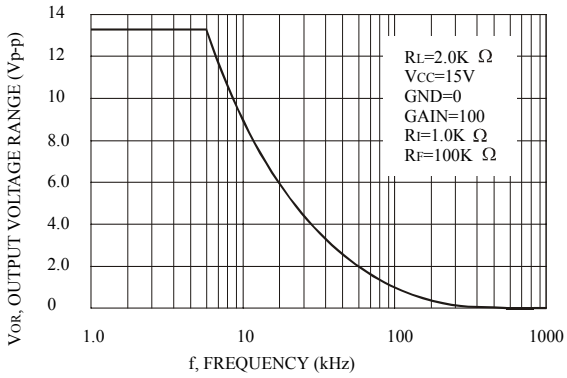


Figure 3. Large-Signal Frequency Response

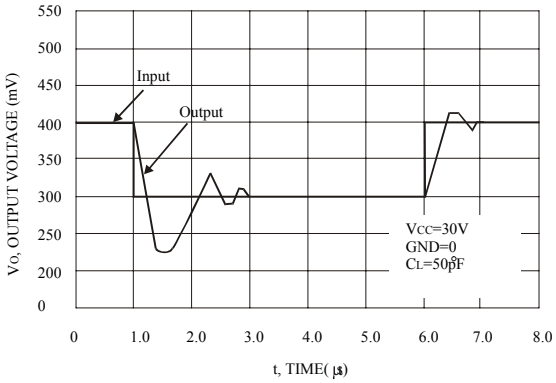


Figure 4. Small-Signal Voltage Follower Pulse Response (Noninverting)

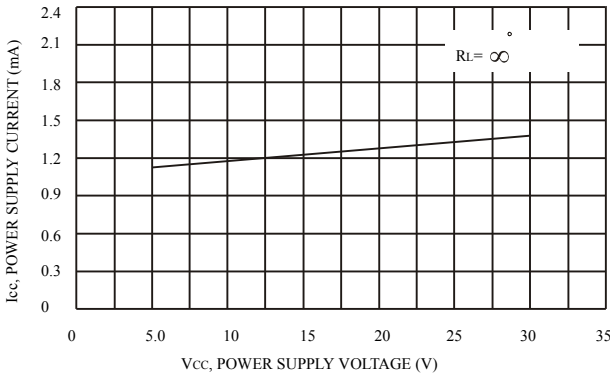


Figure 5. Power Supply Current versus Power Supply Voltage

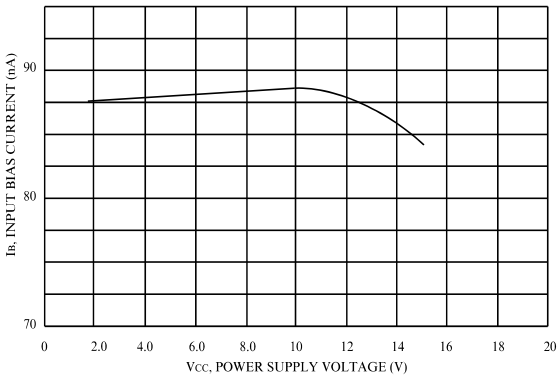


Figure 6. Input Bias Current versus Power Supply Voltage

INTEGRAL

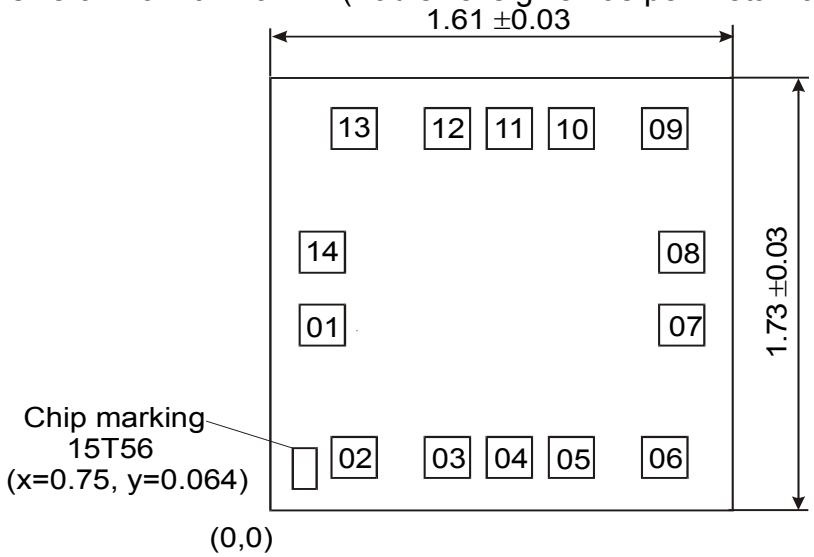
TYPICAL DC ELEKTRICAL CHARACTERISTICS (T_A= +25^{O}C)

Symbol	Parameter	Test Conditions	Value	Unit
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Drift	V_{ICR} =0V, V_{CC}=30V	7.0*	μV/^{O}C
$\Delta I_{IO}/\Delta T$	Input Offset Current Drift	V_{ICR} =0V, V_{CC}=30V	10*	nA/^{O}C
CS	Channel Separation	f=1KHz to 20KHz, V_{CC}=30V	-120	DB

* T_A= 0 ÷to+70^{O}C

CHIP PAD DIAGRAM IZ324

Pad size 0.120 x 0.120 mm (Pad size is given as per metalization layer)



Thickness of chip 0,35±0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	OUT1	0.085	0.680
02	IN1(-)	0.167	0.096
03	IN1(+)	0.558	0.096
04	Vcc	0.745	0.096
05	IN2(+)	0.932	0.096
06	IN2(-)	1.323	0.096
07	OUT2	1.405	0.680
08	OUT3	1.405	0.930
09	IN3(-)	0.932	1.514
10	IN3(+)	0.745	1.514
11	GND	0.558	1.514
12	IN4(+)	0.167	1.514
13	IN4(-)	0.085	1.514
14	OUT4	0.085	0.930