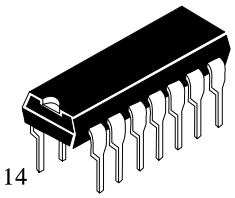
**IN74HC05A**

# Hex Inverter with Open-Drain Outputs

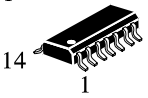
The IN74HC05A is identical in pinout to the LS/ALS05. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

This device contains six independent gates, each of which performs the logic INVERT function. The open-drain outputs require external pull-up resistors for proper logical operation. They may be connected to other open-drain outputs to implement active-high wired-AND functions.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices




N SUFFIX
PLASTIC



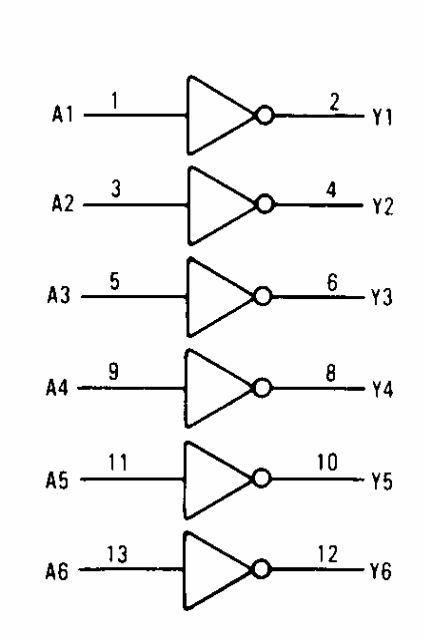

D SUFFIX
SOIC

**ORDERING INFORMATION**

| | |
|---|---|
| IN74HC05AN | Plastic |
| IN74HC05AD | SOIC |
| IZ74HC05AZ | Chip |

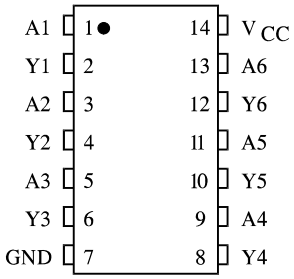
$T_A$ = -55° to 125° C for all packages

## LOGIC DIAGRAM




PIN 14 =$V_{CC}$
PIN 7 = GND

## PIN ASSIGNMENT




## FUNCTION TABLE

| Inputs | Output |
|---|---|
| A | Y |
| L | Z |
| H | L |

Z = High Impedance

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | -1.5 to $V_{CC}$ +1.5 | V |
| $V_{OUT}$ | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC}$ +0.5 | V |
| $I_{IN}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{OUT}$ | DC Output Current, per Pin | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±50 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic DIP**<br>SOIC Package** | 750<br>500 | mW |
| Tstg | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | 2.0 | 6.0 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | -55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | $V_{CC}$ =2.0 V<br>$V_{CC}$ =4.5 V<br>$V_{CC}$ =6.0 V | 0<br>0<br>0 | 1000<br>500<br>400 | ns |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{IN}$ and $V_{OUT}$ should be constrained to the range GND≤($V_{IN}$ or $V_{OUT}$)≤$V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 25 °C to -55°C | ≤85 °C | ≤125 °C | |
| $V_{IL}$ | Low -Level Input Voltage | $V_{OUT}$ = $V_{CC}$ or 0 V<br>$\|I_{OUT}\| \leq \pm 0.5\ \mu A$ (□= -55 to 25°C) $\|I_{OUT}\| \leq \pm 5.0\ \mu A$ (□= 85°C) $\|I_{OUT}\| \leq \pm 10\ \mu A$ (□= 125°C) | 2.0<br>4.5<br>6.0 | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | V |
| $V_{IH}$ | High-Level Input Voltage | $V_{OUT} \leq 0.1$ V<br>$\|I_{OUT}\| \leq 20\ \mu A$ | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V |
| $V_{OL}$ | Low - Level Output Voltage | $V_{IN}$=$V_{IH}$<br>$\|I_{OUT}\| \leq 20\ \mu A$ | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V |
| | | $V_{IN}$=$V_{IH}$<br>$\|I_{OUT}\| \leq 4.0$ mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| | | $V_{IN}$=$V_{IH}$<br>$\|I_{OUT}\| \leq 5.2$ mA | 6.0 | 0.26 | 0.33 | 0.40 | |
| $I_{IL}$ | Input Leakage Current | $V_{IL}$= GND | 6.0 | -0.1 | -1.0 | -1.0 | μA |
| $I_{IH}$ | Input Leakage Current | $V_{IH}$=$V_{CC}$ | 6.0 | -0.1 | -1.0 | -1.0 | μA |
| $I_{CC}$ | Quiescent Supply Current (per Package) | $V_{IL}$=GND<br>$V_{IH}$=$V_{CC}$<br>$I_{OUT}$=0 μA | 6.0 | 1.0 | 10 | 40 | μA |
| $I_{OZL}$ | Three-State Leakage Current | $V_{IN}$= $V_{IL}$ or $V_{IH}$<br>$V_{OUT}$= GND | 6.0 | -0.5 | -5.0 | -10 | μA |
| $I_{OZH}$ | Three-State Leakage Current | $V_{IN}$= $V_{IL}$ or $V_{IH}$<br>$V_{OUT}$= $V_{CC}$ | 6.0 | -0.5 | -5.0 | -10 | μA |

## AC ELECTRICAL CHARACTERISTICS ($C_L$=50pF, Input $t_r$=$t_f$=6.0 ns)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 25 °C to -55°C | ≤85 °C | ≤125 °C | |
| $t_{PLZ}$, $t_{PZL}$ | Propagation Delay, Input A to Output Y (Figures 1 and 2) | $V_{IL}$ = GND<br>$V_{IH}$ = $V_{CC}$<br>$t_{LH}$ = $t_{HL}$ = 6 ns<br>$C_L$ = 50 pF | 2.0<br>4.5<br>6.0 | 120<br>24<br>20 | 150<br>30<br>26 | 180<br>36<br>31 | ns |
| $t_{THL}$ | Output Transition Time, Any Output (Figures 1 and 2) | $V_{IL}$ = GND<br>$V_{IH}$ = $V_{CC}$<br>$t_{LH}$ = $t_{HL}$ = 6 ns<br>$C_L$ = 50 pF | 2.0<br>4.5<br>6.0 | 75<br>15<br>13 | 95<br>19<br>16 | 110<br>22<br>19 | ns |
| $C_{IN}$ | Input Capacitance | | | 10 | 10 | 10 | pF |
| $C_{OUT}$ | Three-State Output Capacitance (Output in High-Impedance State) | | | 10 | 10 | 10 | pF |

| | | | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Gate)<br>Used to determine the no-load dynamic power consumption:<br>$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ | Typical @25°C, $V_{CC}$=5.0 V<br>8.0 | pF |

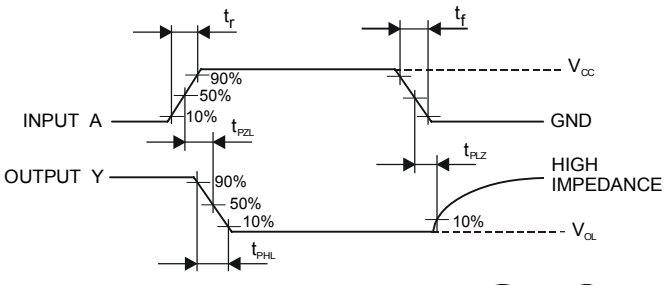



**Figure 1. Switching Waveforms**

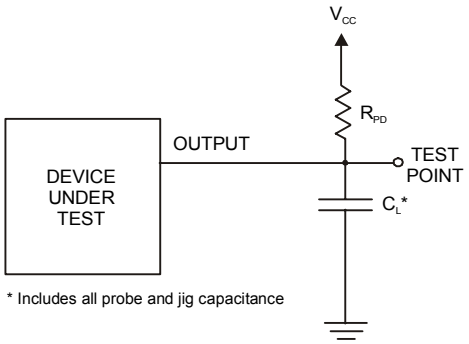



**Figure 2. Test Circuit**

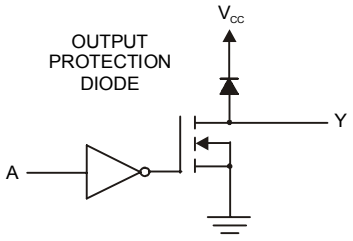
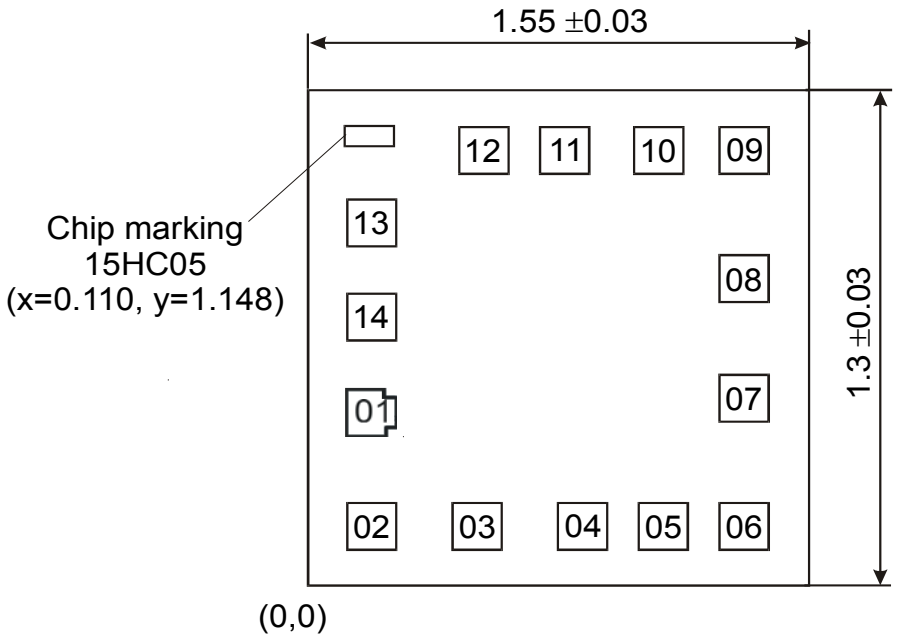



**Figure 3. Expanded Logic Diagram (1/6 of the Device)**

## CHIP PAD DIAGRAM IZ74HC05A




Pad size 0.106 x 0.106 mm (Pad size is given as per passivation layer)
Thickness of chip 0,46±0,02 mm

## PAD LOCATION

| Pad No | Symbol | X | Y |
|---|---|---|---|
| 01 | A1 | 0.126 | 0.492 |
| 02 | Y1 | 0.136 | 0.122 |
| 03 | A2 | 0.432 | 0.112 |
| 04 | Y2 | 0.793 | 0.112 |
| 05 | A3 | 0.948 | 0.112 |
| 06 | Y3 | 1.312 | 0.112 |
| 07 | GND | 1.312 | 0.471 |
| 08 | Y4 | 1.312 | 0.643 |
| 09 | A4 | 1.312 | 1.062 |
| 10 | Y5 | 1.107 | 1.062 |
| 11 | A5 | 0.747 | 1.062 |
| 12 | Y6 | 0.492 | 1.062 |
| 13 | A6 | 0.126 | 0.941 |
| 14 | Vcc | 0.126 | 0.747 |