

IN74HC161A

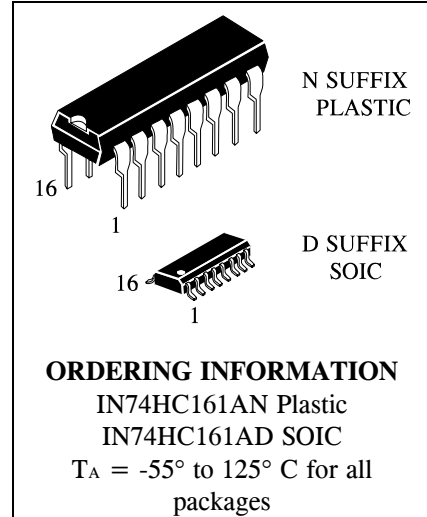
Presettable Counters
High-Performance Silicon-Gate CMOS

The IN74HC161A is identical in pinout to the LS/ALS161. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

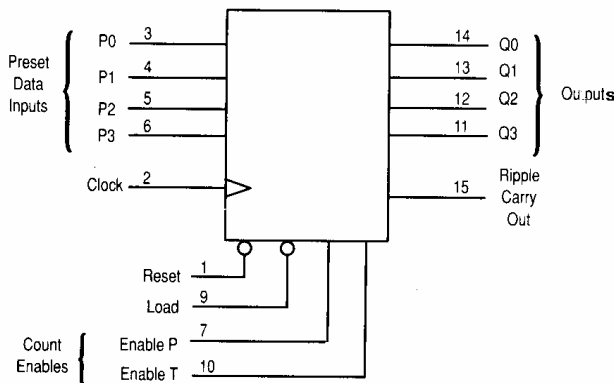
The IN74HC161A is programmable 4-bit synchronous counter that feature parallel Load, asynchronous Reset, a Carry Output for cascading and count-enable controls.

The IN74HC161A is binary counter with asynchronous Reset.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices



LOGIC DIAGRAM



PIN 16 = V_{CC}
 PIN 8 = GND

PIN ASSIGNMENT

Reset	1	16	V _{CC}
Clock	2	15	Ripple Carry Out
P0	3	14	Q0
P1	4	13	Q1
P2	5	12	Q2
P3	6	11	Q3
Enable P	7	10	Enable T
GND	8	9	Load

FUNCTION TABLE

Inputs					Outputs				Function
Reset	Load	Enable P	Enable T	Clock	Q0	Q1	Q2	Q3	
L	X	X	X	X	L	L	L	L	Reset to "0"
H	L	X	X	⎓	P0	P1	P2	P3	Preset Data
H	H	X	L	⎓	No change				No count
H	H	L	X	⎓	No change				No count
H	H	H	H	⎓	Count up				Count
H	X	X	X	⎓	No change				No count

X=don't care
 P0,P1,P2,P3 = logic level of Data inputs
 Ripple Carry Out = Enable T • Q0 • Q1 • Q2 • Q3

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package +	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			
	V _{CC} = 2.0 V	0	1000	ns
	V _{CC} = 4.5 V	0	500	
	V _{CC} = 6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	4.5	3.98	3.84	3.7	
6.0	5.48	5.34	5.2				
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (Figures 1,6)	2.0	6	5	4	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH}	Maximum Propagation Delay Clock to Q (Figures 1,6)	2.0	120	160	200	ns
		4.5	20	23	28	
		6.0	16	20	22	
t _{PHL}	Maximum Propagation Delay Reset to Q (Figures 2 and 6)	2.0	145	185	320	ns
		4.5	22	25	30	
		6.0	18	20	23	
t _{PLH}	Maximum Propagation Delay Enable T to Ripple Carry Out (Figures 3,6)	2.0	110	150	190	ns
		4.5	16	18	20	
		6.0	14	15	17	
t _{PHL}	Maximum Propagation Delay Enable T to Ripple Carry Out (Figures 2,6)	2.0	135	175	210	ns
		4.5	18	20	22	
		6.0	15	16	20	
t _{PLH}	Maximum Propagation Delay Clock to Ripple Carry Out (Figures 1,6)	2.0	120	160	200	ns
		4.5	22	27	30	
		6.0	18	22	25	
t _{PHL}	Maximum Propagation Delay Reset to Ripple Carry Out (Figures 2,6)	2.0	145	185	220	ns
		4.5	22	28	35	
		6.0	20	24	28	
t _{PLH}	Maximum Propagation Delay Reset to Ripple Carry Out (Figures 2,6)	2.0	155	190	230	ns
		4.5	22	26	30	
		6.0	18	22	25	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{IN}	Maximum Input Capacitance	-	10	10	10	pF
C _{PD}	Power Dissipation Capacitance (Per Gate)	Typical @25°C, V _{CC} =5.0 V				pF
	Used to determine the no-load dynamic power consumption: $P_D = C_{PD}V_{CC}^2f + I_{CC}V_{CC}$	30				

TIMING REQUIREMENTS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t _{SU}	Minimum Setup Time, Preset Data Inputs to Clock (Figure 4)	2.0	40	60	80	ns
		4.5	15	20	30	
		6.0	12	18	20	
t _{SU}	Minimum Setup Time, Load to Clock (Figure 4)	2.0	60	75	90	ns
		4.5	15	20	30	
		6.0	12	18	20	
t _{SU}	Minimum Setup Time, Enable T or Enable P to Clock (Figure 5)	2.0	80	95	110	ns
		4.5	20	25	35	
		6.0	17	23	25	
t _H	Minimum Hold Time, Clock to Load or Preset Data Inputs (Figure 4)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t _H	Minimum Hold Time, Clock to Enable T or Enable P (Figure 5)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t _{REC}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	80	95	110	ns
		4.5	15	20	26	
		6.0	12	17	23	
t _{REC}	Minimum Recovery Time, Load Inactive to Clock (Figure 4)	2.0	80	95	110	ns
		4.5	15	20	26	
		6.0	12	17	23	
t _W	Minimum Pulse Width, Clock (Figure 1)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t _W	Minimum Pulse Width, Reset (Figure 2)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

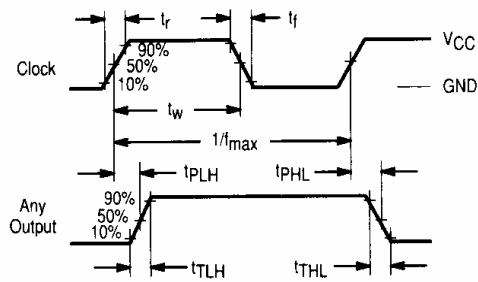


Figure 1. Switching Waveforms

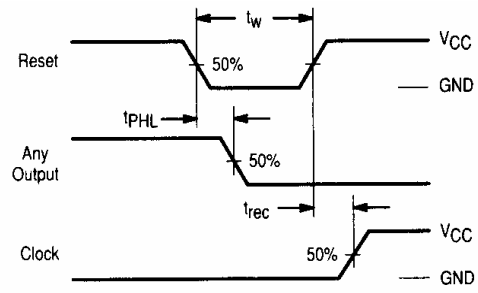


Figure 2. Switching Waveforms

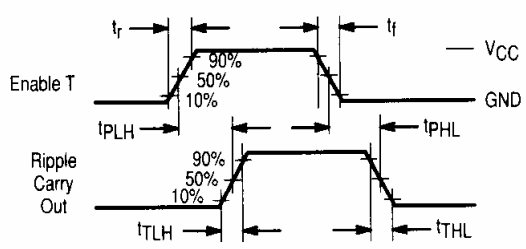


Figure 3. Switching Waveforms

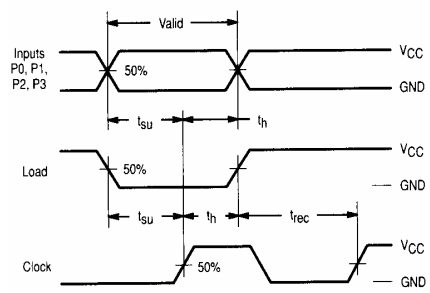


Figure 4. Switching Waveforms

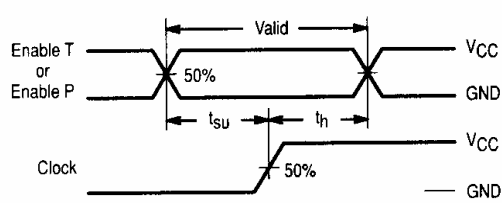
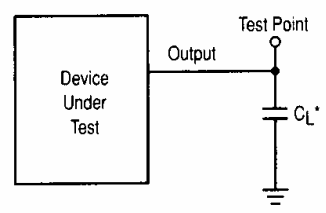
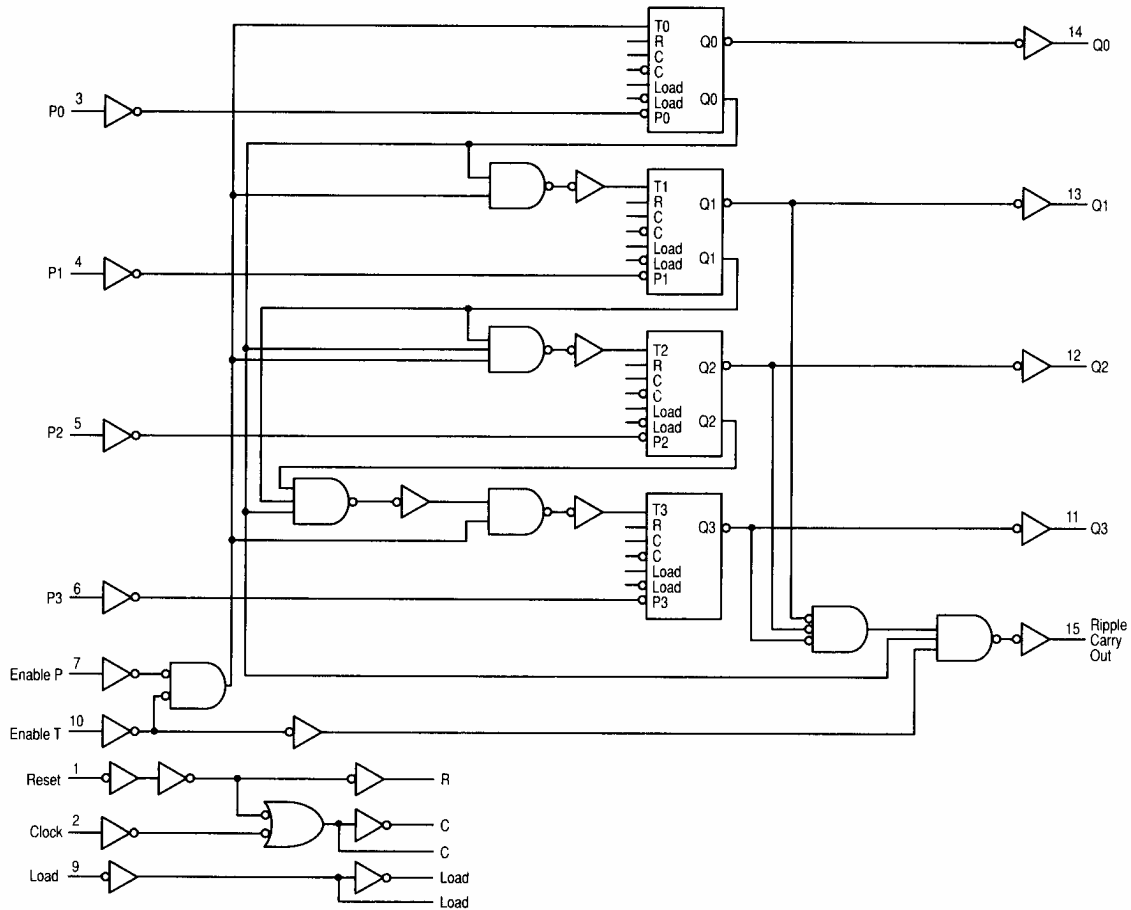


Figure 5. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

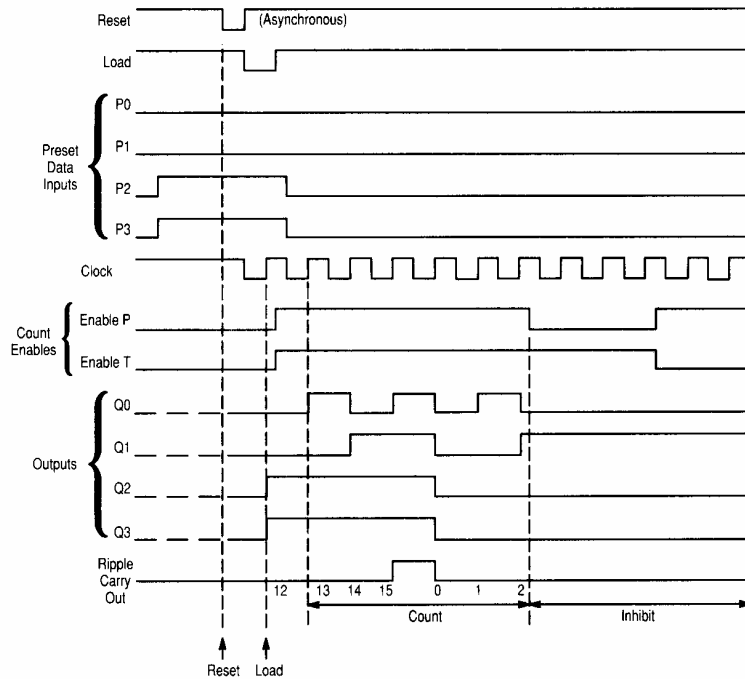


V_{CC} = Pin 16
 GND = Pin 8

The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

Figure 7. Expanded logic diagram

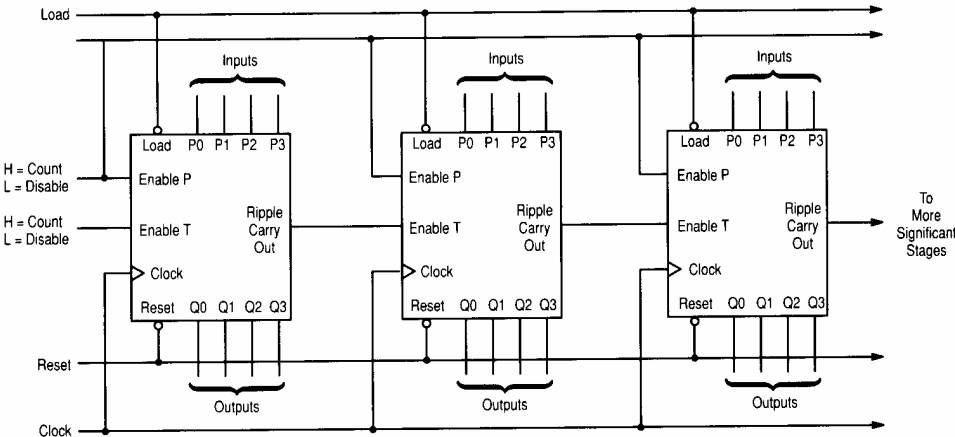


Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

Figure 8. Timing Diagram

TYPICAL APPLICATIONS CASCADING



Note: When used in these cascaded configurations the clock f_{max} guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and clock.

Figure 9. N-Bit Synchronous Counters

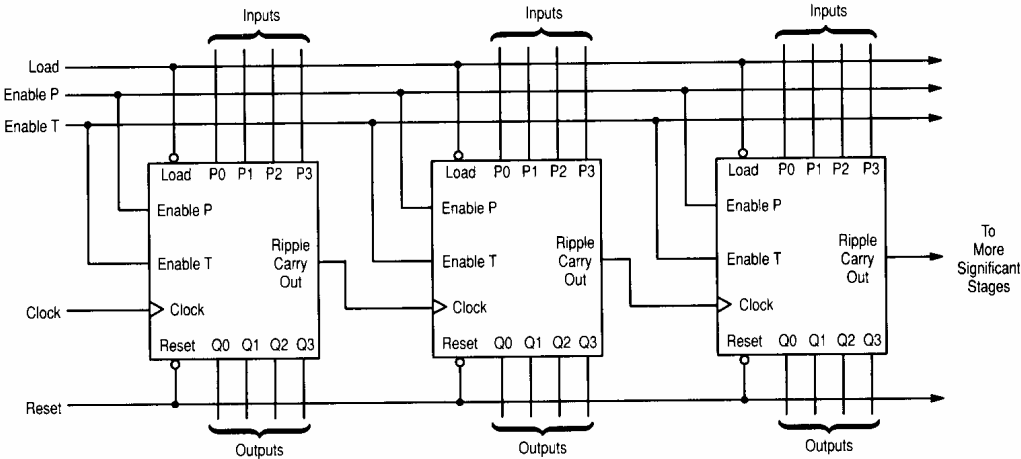


Figure 10. Nibble Ripple Counter