

IN74AC373

Octal 3-State Noninverting Transparent Latch

The IN74AC373 is identical in pinout to the LS/ALS373, HC/HCT373. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALS outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A; 0.1 μ A @ 25°C
- High Noise Immunity Characteristic of CMOS Devices
- Outputs Source/Sink 24 mA

N SUFFIX PLASTIC

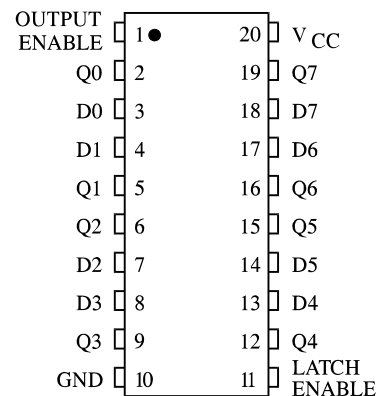
DW SUFFIX SOIC

ORDERING INFORMATION

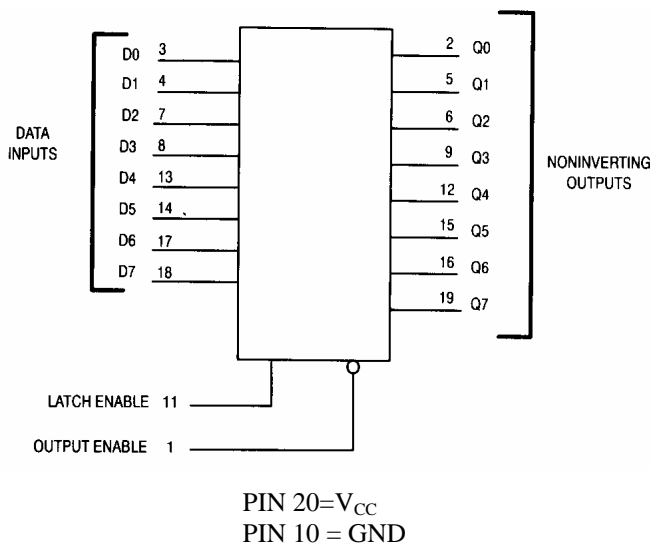
IN74AC373N	Plastic
IN74AC373DW	SOIC
IZ74AC373	Chip

$T_A = -45^\circ$ to 85° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

**Derating - Plastic DIP: - 10 mW/°C from 65° to 85°C
SOIC Package: - 7 mW/°C from 65° to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _J	Junction Temperature (PDIP)		140	°C	
T _A	Operating Temperature, All Package Types	-45	+85	°C	
I _{OH}	Output Current - High		-24	mA	
I _{OL}	Output Current - Low		24	mA	
t _r , t _f	Input Rise and Fall Time * (except Schmitt Inputs)	V _{CC} =3.0 V V _{CC} =4.5 V V _{CC} =5.5 V	0 0 0	150 40 25	ns/V

* V_{IN} from 30% to 70% V_{CC}

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limits		Unit	
				25 °C	-45°C to 85°C		
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V	3.0	2.1	2.1	V	
			4.5	3.15	3.15		
			5.5	3.85	3.85		
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V	3.0	0.9	0.9	V	
			4.5	1.35	1.35		
			5.5	1.65	1.65		
V _{OH}	Minimum High-Level Output Voltage	I _{OUT} ≤ -50 μA	3.0	2.9	2.9	V	
			4.5	4.4	4.4		
			5.5	5.4	5.4		
		*V _{IN} =V _{IH} or V _{IL}					
		I _{OH} =-12 mA	3.0	2.56	2.46		
		I _{OH} =-24 mA	4.5	3.86	3.76		
I _{OH} =-24 mA	5.5	4.86	4.76				
V _{OL}	Maximum Low-Level Output Voltage	I _{OUT} ≤ 50 μA	3.0	0.1	0.1	V	
			4.5	0.1	0.1		
			5.5	0.1	0.1		
		*V _{IN} =V _{IH} or V _{IL}					
		I _{OL} =12 mA	3.0	0.36	0.44		
		I _{OL} =24 mA	4.5	0.36	0.44		
I _{OL} =24 mA	5.5	0.36	0.44				
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	5.5	±0.1	±1.0	μA	
I _{OZ}	Maximum Three-State Leakage Current	V _{IN} (OE)= V _{IH} or V _{IL} V _{IN} =V _{CC} or GND V _{OUT} =V _{CC} or GND	5.5	±0.5	±5.0	μA	
I _{OLD}	**Minimum Dynamic Output Current	V _{OLD} =1.65 V Max	5.5		75	mA	
I _{OHD}	**Minimum Dynamic Output Current	V _{OHD} =3.85 V Min	5.5		-75	mA	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND	5.5	8.0	80	μA	

* All outputs loaded; thresholds on input associated with output under test.

**Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @3.0 V are guaranteed to be less than or equal to the respective limit @5.5 V V_{CC}

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, $t_r=t_f=3.0\text{ ns}$)

Symbol	Parameter	V_{CC}^* V	Guaranteed Limits				Unit
			25 °C		-45°C to 85°C		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay, Input D to Q (Figure 1)	3.3 5.0	1.5 1.5	13.5 9.5	1.5 1.5	15.0 10.5	ns
t_{PHL}	Propagation Delay, Input D to Q (Figure 1)	3.3 5.0	1.5 1.5	13.0 9.5	1.5 1.5	14.5 10.5	ns
t_{PLH}	Propagation Delay, Latch Enable to Q (Figure 2)	3.3 5.0	1.5 1.5	13.5 9.5	1.5 1.5	15.0 10.5	ns
t_{PHL}	Propagation Delay, Latch Enable to Q (Figure 2)	3.3 5.0	1.5 1.5	12.5 9.5	1.5 1.5	14.0 10.5	ns
t_{PZH}	Propagation Delay, Output Enable to Q (Figure 3)	3.3 5.0	1.5 1.5	11.5 8.5	1.0 1.0	13.0 9.5	ns
t_{PZL}	Propagation Delay, Output Enable to Q (Figure 3)	3.3 5.0	1.5 1.5	11.5 8.5	1.0 1.0	13.0 9.5	ns
t_{PHZ}	Propagation Delay, Output Enable to Q (Figure 3)	3.3 5.0	1.5 1.5	12.5 11.0	1.0 1.0	14.5 12.5	ns
t_{PLZ}	Propagation Delay, Output Enable to Q (Figure 3)	3.3 5.0	1.5 1.5	11.5 8.5	1.0 1.0	12.5 10.0	ns
C_{IN}	Maximum Input Capacitance	5.0	4.5		4.5		pF

C_{PD}	Power Dissipation Capacitance	Typical @25°C, $V_{CC}=5.0\text{ V}$		pF
		40		

*Voltage Range 3.3 V is 3.3 V \pm 0.3 V

Voltage Range 5.0 V is 5.0 V \pm 0.5 V

TIMING REQUIREMENTS($C_L=50\text{pF}$, Input $t_r=t_f=3.0\text{ ns}$)

Symbol	Parameter	V_{CC}^* V	Guaranteed Limits		Unit	
			25 °C			-45°C to 85°C
			Min	Max		Min
t_s	Minimum Setup Time, Input D to Latch Enable (Figure 4)	3.3 5.0	5.5 4.0	6.0 4.5	ns	
t_h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	3.3 5.0	1.0 1.0	1.0 1.0	ns	
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	3.3 5.0	5.5 4.0	6.0 4.5	ns	

*Voltage Range 3.3 V is 3.3 V \pm 0.3 V

Voltage Range 5.0 V is 5.0 V \pm 0.5 V

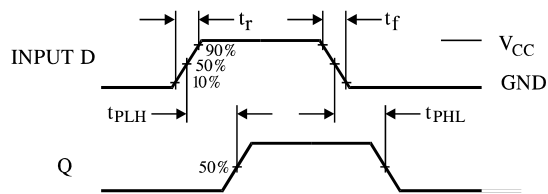


Figure 1. Switching Waveforms

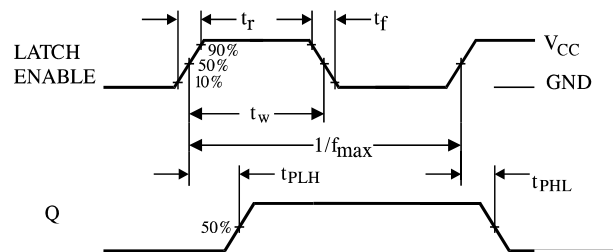


Figure 2. Switching Waveforms

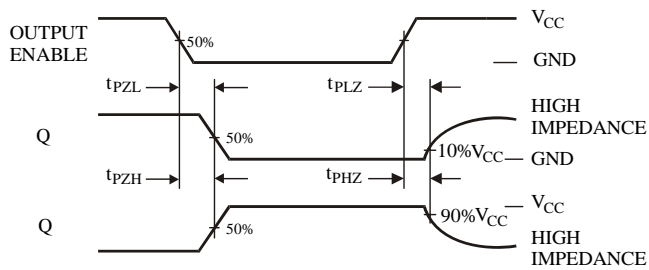


Figure 3. Switching Waveforms

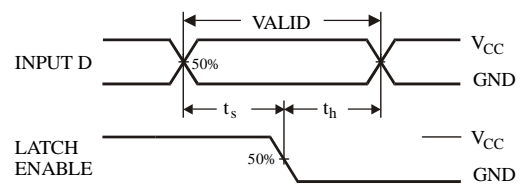
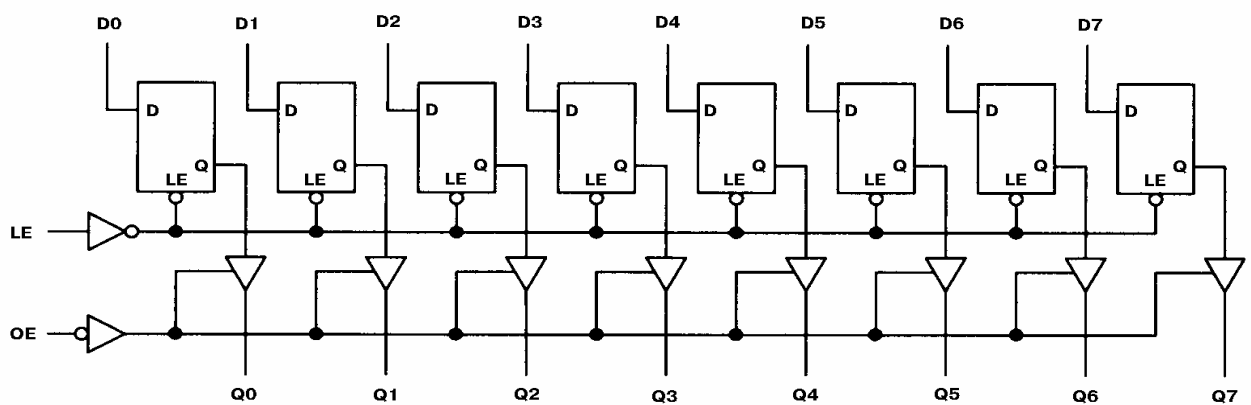
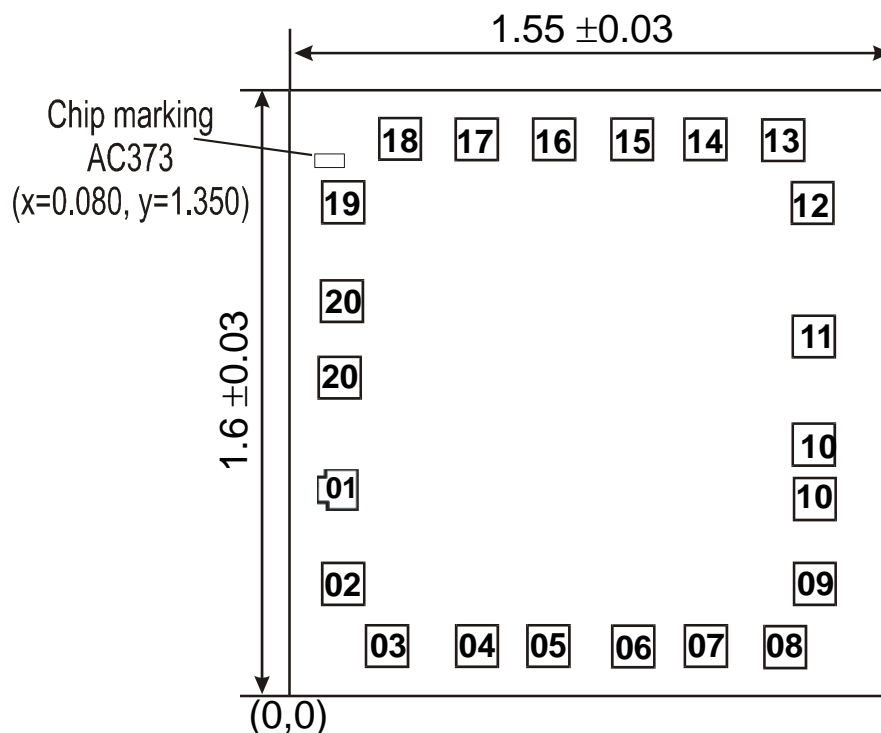


Figure 4. Switching Waveforms

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM IZ74AC373



Pad size 0.120 x 0.120 mm (Pad size is given as per metallization layer)

Thickness of chip 0,46±0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	OE	0.100	0.510
02	Q0	0.100	0.280
03	D0	0.160	0.100
04	D1	0.450	0.100
05	Q1	0.636	0.100
06	Q2	0.810	0.100
07	D2	0.990	0.100
08	D3	1.280	0.100
09	Q3	0.339	0.280
10	GND	1.330/1.330	0.470/0.630
11	LE	1.330	0.970
12	Q4	1.330	1.200
13	D4	1.280	1.380
14	D5	0.990	1.380
15	Q5	0.810	1.380
16	Q6	0.630	1.380
17	D6	0.450	1.380
18	D7	0.160	1.380
19	Q7	0.100	1.200
20	Vcc	0.100/0.100	1.020/0.860