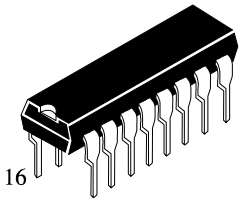
14-STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDER AND OSCILLATOR

High-Voltage Silicon-Gate CMOS

The IW4060B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-Q's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of OSC In (and OSC Out). Schmitt trigger action on the input-pulse line permits unlimited input-pulse rise and fall times.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):

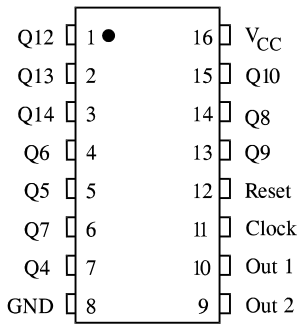
1.0 V min @ 5.0 V supply
2.0 V min @ 10.0 V supply
2.5 V min @ 15.0 V supply



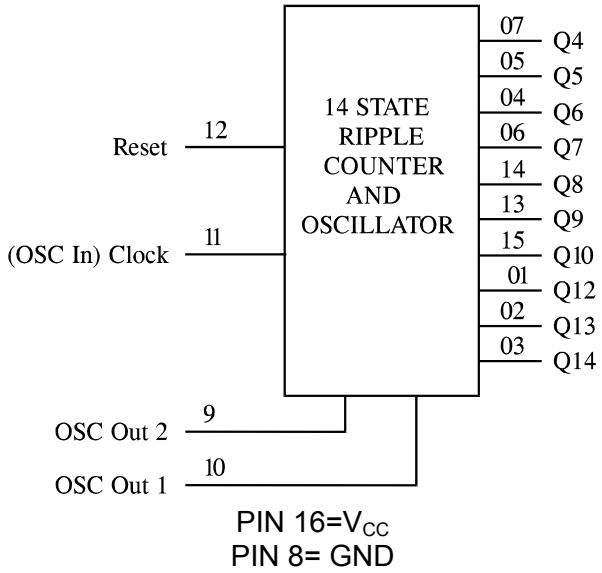
ORDERING INFORMATION

IW4060BN Plastic
IW4060BD SOIC
T_A = -55° to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16=V_{CC}
PIN 8= GND

FUNCTION TABLE

Inputs		Outputs
Osc In	Reset	Q
⎍	L	No change
⎎	L	Advance to next state
X	H	All Outputs are low

X = don't care

INTEGRAL

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}= 0.5 V or V_{CC} - 0.5V V_{OUT}= 1.0 V or V_{CC} - 1.0 V V_{OUT}= 1.5 V V_{CC} - 1.5V	5.0 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}= 0.5 V or V_{CC} - 0.5V V_{OUT}= 1.0 V or V_{CC} - 1.0 V V_{OUT}= 1.5 V V_{CC} - 1.5V	5.0 10 15	1.5 3 4	1.5 3 4	1.5 3 4	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0 10 15 20	5 10 20 100	5 10 20 100	150 300 600 3000	μA
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC} U_{OL}=0.4 V U_{OL}=0.5 V U_{OL}=1.5 V	 5.0 10 15	 0.64 1.6 4.2	 0.51 1.3 3.4	 0.36 0.9 2.4	mA
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC} U_{OH}=2.5 V U_{OH}=4.6 V U_{OH}=9.5 V U_{OH}=13.5 V	 5.0 5.0 10 15	 -2 -0.64 -1.6 -4.2	 -1.6 -0.51 -1.3 -3.4	 -1.15 -0.36 -0.9 -2.4	mA

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=200kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			≥-55 °C	25°C	≤125 °C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figure 1)	5.0 10 15	3.5 8 12	3.5 8 12	1.75 4 6	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q4 (Figure 1)	5.0 10 15	740 300 200	740 300 200	1480 600 400	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Q_n to Q_{n+1} (Figure 2)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figure 3)	5.0 10 15	360 160 100	360 160 100	720 320 200	ns
t_{THL}, t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS(C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			≥-55 °C	25°C	≤125 °C	
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0 10 15	100 40 30	100 40 30	200 80 60	ns
t_w	Minimum Pulse Width, Reset (Figure 3)	5.0 10 15	120 60 40	120 60 40	240 120 80	ns
t_f, t_r	Maximum Input Rise and Fall Times (Figure 1)	5.0 10 15	Unlimited			ns

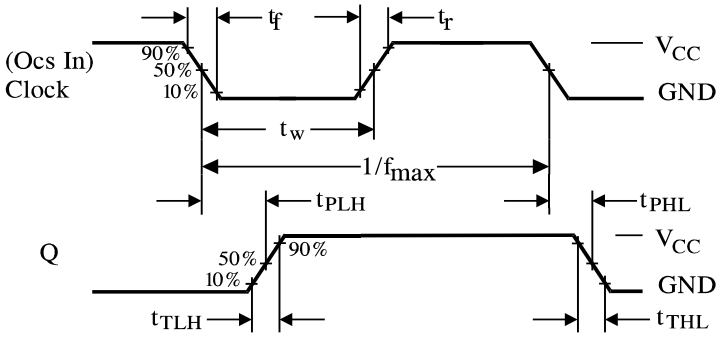


Figure 1. Switching Waveforms

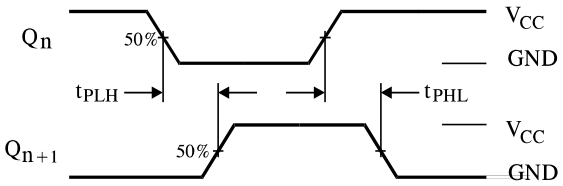


Figure 2. Switching Waveforms

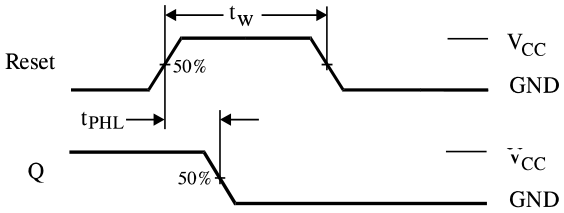
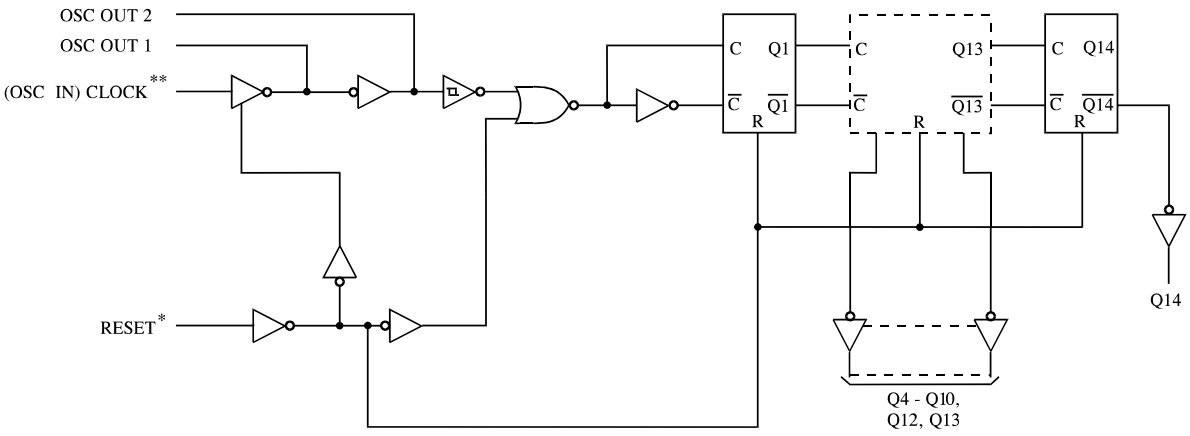


Figure 3. Switching Waveforms

EXPANDED LOGIC DIAGRAM



* R = HIGH DOMINATES (RESETS ALL STAGES)
** COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE - GOING TRANSITION OF CLOCK (AND OSC OUT)