ICs ILE4270G, ILE4270S OF POWER VOLTAGE REGULATOR 5 V/550MA WITH LOW RESIDUAL VOLTAGE (FUNCTIONAL EQUVIVALENT TLE4270G BY SIEMENS)

ICs perform stabilizing of output voltage 5 V with 2% accuracy in the range of input voltages from 5.5 to 26 V, providing a load current not less 550 mA with residual voltage less than 0.7 V.
The spread of the output voltage is provided by adjustment of the reference voltage by means of fusion of diode jumpers on the crystal.

Maximum input voltage 42 V (65 V during the time t $\leq$ 400 ms).
Maximum output current when a short circuit, more than 650 mA.

ICs are realized in 5-pin plastic packages of P-TO263-5-1 and P-TO220-5-12.

ICs are suitable for use in power supply in electronic equipment including automotive electronics.

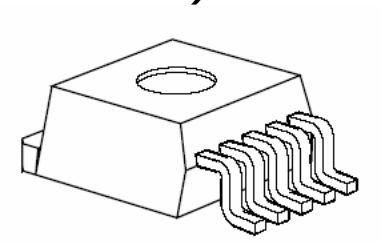


Fig. 1 – View of IC in P-TO263-5-1 package

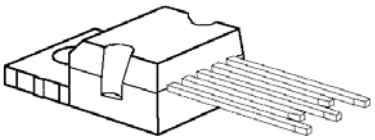


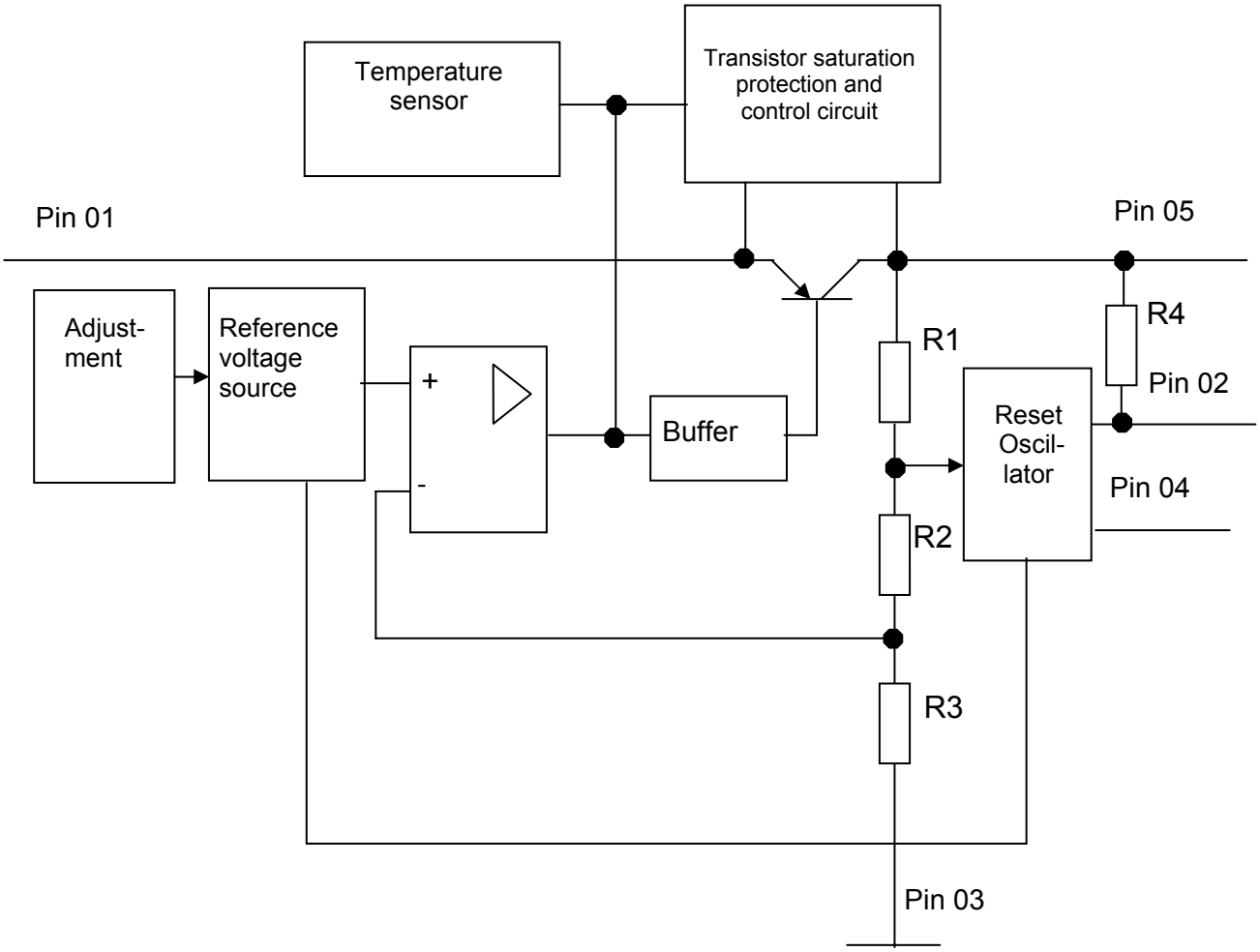
Fig. 2 – View of IC in P-TO220-5-12 package

Features:

- High precision of output voltage 5V $\pm$ 2%;
- Low residual voltage;
- Imbedded overtemperature protection;
- Reverse polarity protection ;
- Very low consumption current;
- Input voltage up to 42V;
- Overvoltage protection up to 65V ($\leq$400mc);
- Short-circuit proof;
- Suitable for use in automotive electronics;
- - ESD protection up to 2000 V;
- Adjustable reset time
- Junction temperature range from minus 40 to +125°C;

Table 1 Pin description table

Pin number	Pad number	Symbol	Description
01	01	I	Input
02	07	RO	Reset oscillator output
03	09	GND	Common
04	10	D	Output of reset signal delay
05	12, 13	Q	Output
-	02-06, 08, 11	-	Not bonded



R1 – R4 – resistors

Fig.3 Block diagramm

Table 2 Absolute maximum ratings

Symbol	Parameter	Norm		Unit
		Min	Max	
U_I	Input voltage	-42	46	V
		-	65*	
I_I	Input current	-	Internally limited	mA
U_Q	Output voltage	-1.0	16	V
I_Q	Output current	-	Internally limited	mA
I_{GND}	GND pin current	-0.5	-	A
U_R	RO pin voltage	-0.3	7.0	V
I_R	RO pin current	-	Internally limited	A
U_D	D pin voltage	-0.3	7.0	V
I_D	D pin current	-	Internally limited	A
Tj	Junction temperature	-	150	°C
Tstg	Storage temperature (ambient)	-50	150	°C
R_{TJC}	Thermal resistance junction-case	-	6.0	°C/W
R_{TJA}	Thermal resistance junction-ambient	-	70	°C/W

* Effect time t ≤ 400 mc

Table 3 Recommended operation mode

Symbol	Parameter	Norm		Unit
		Min	Max	
U_I	Input voltage	U_Q + 0.7 B	46	V
I_I	Input current	-5.0	Internally limited	mA
U_Q	Output voltage	4.9	5.1	V
I_Q	Output current	-5.0	Internally limited	mA
U_R	RO pin voltage	0	-	V
I_R	RO pin current	-	Internally limited	A
I_D	D pin current	-	Internally limited	A
Tj	Junction temperature	-40*	125	°C
R_{TJC}	Thermal resistance junction-case	-	6.0	°C/W
R_{TJA}	Thermal resistance junction-ambient (without heat sink)	-	70	°C/W

Table 3 continued

Note – Absolute maximum power P_{tot},mW, dissipated by IC at the ambient temperature T_A, is to be determined as

$Ptot = (125 - T_A) / R_{TJA}$ (1)

where 125 – junction absolute maximum operating temperature, °C

* R_{TJA} - thermal resistance "junction – ambient" (for IC without additional external heat sink), °C /W.

For IC with additional external heat sink

$R_{TJA} = R_{TJC} + R_{TJCA}$, (2)

where R_{TJC} – IC thermal resistance "junction-case", °C /W.

Thermal resistance "case-ambient" $R_{th\ ca}$ of the designed IC is determined by the design of heat sink and specified by IC consumer.

Used heat sink, application mode (consumed power) and ambient temperature have to ensure junction temperature nor more than $T_J \leq +125$ °C.

* Ambient temperature is indicated

Table 4 – Electric parameters - 40 °C *≤ T_J ≤ 125 °C (unless otherwise specified)

Symbol	Parameter	Mode	Norm		Unit
			Min	Max	
U_Q	Output voltage	6.0 V ≤ U_I ≤ 26 v -5.0 mA ≤ I_Q ≤ - 550 mA	4.9	5.1	V
		26 V ≤ U_I ≤ 36 V I_Q ≤ - 300 mA	4.9	5.1	
I_{Qmax}	Maximum output current	U_Q = 0 V U_I = 13.5 V	650	-	mA
Iq	Consumption current (Iq = I_I - I_Q)	U_I = 13.5 V, I_Q = -5.0 mA	-	1.5	mA
		U_I = 13.5 V, I_Q = -550 mA	-	75	
		U_I = 5.0 V, I_Q = -550 mA	-	90	
Udr	Drop voltage	U_I = 13.5 V, I_Q = -550 mA	-	700	mV
$\Delta U_{Q(I)}$	Load current regulation of output voltage	U_I =6.0 V -5.0 mA ≤ I_Q≤ -550mA	-	50	mV
$\Delta U_{Q(U)}$	Supply (input) voltage regulation of output voltage	6.0 V ≤ U_I ≤ 26 V I_Q = -5.0 mA	-	25	mV
Reset oscillator parameters					
U_{RT}	Switching reset threshold voltage (pin 05)	I_Q = -5.0 mA	4.5	4.8	V
U_{ROH}	High level reset output voltage	U_I = 13.5 V, I_Q = -5.0 mA	4.5	-	V

Table 4 continued

Symbol	Parameter	Mode	Norm		Unit
			Min	Max	
U_{ROL}	Low level reset output voltage	U_Q =4.4 V, U_I = 4.4 V I_R = 3.0 mA	-	400	mV
R	Circuit resistence	Connection directly to Q	18	46	kΩ
U_{DRL}	Switching threshold of "Reset" output into low level	$U_Q < U_{RT}$	0.2	0.8	V
U_{DU}	Switching threshold of "Reset" output into high level	-	1.4	2.3	V
Id	Charge current	U_D = 1.5 V	8.0	25	μA
t_{RR}	"Reset" output actuating time	C_D = 100 nF	-	3.0	μs
Overvoltage protection					
$U_{I,0V}$	Switching OFF voltage		42	46	V

Notes

1. Parameters specified in the table are guaranteed for the constant junction temperature Tj. Measurement of parameters should be conducted by means of pulse technique.

2. Minus sign before current value indicates current direction only (drain current). The absolute value of the measured current was adopted as value of current.

3. Measurement of electrical parameters is carried out with connection of input capacitors C_I = 1000 μF, C_2 = 470 nF and output capacitor C_Q = 22 μF.

4 "Reset" output is in low level state at 1.0 V < U_Q < U_{RT}

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∗ Ambient temperature is indicated

Table 5 Typical electrical parameters
(-40 °C ≤ T_J ≤ 125 °C, unless otherwise specified)

Parameter, unit	Symbol	Measurement mode	Typical value
Switching delay time, mc	t_d	C_d = 100 nF	13
Low reset voltage, mV	U_{ROL}	R_{intern} = 30 kΩ 1.0 V ≤ U_Q ≤ 4.5 V	60
Ripple rejection ratio, dB	PSRR	f_r = 100 Hz, U_r = 0.5 U_{SS}	54
Notes: Testing of electrical characteristics is carried out in compliance with connection circuit given in Annex A			

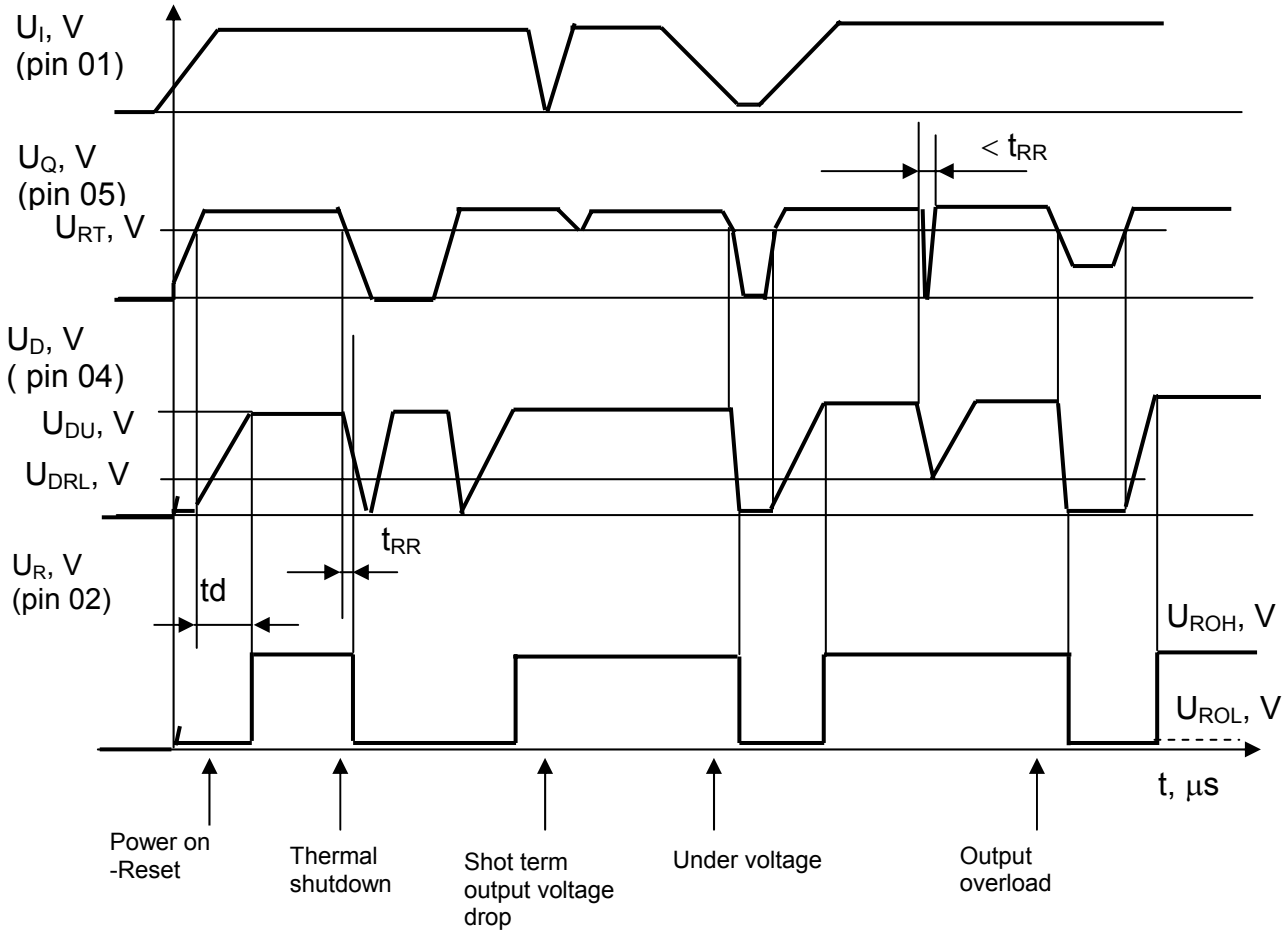
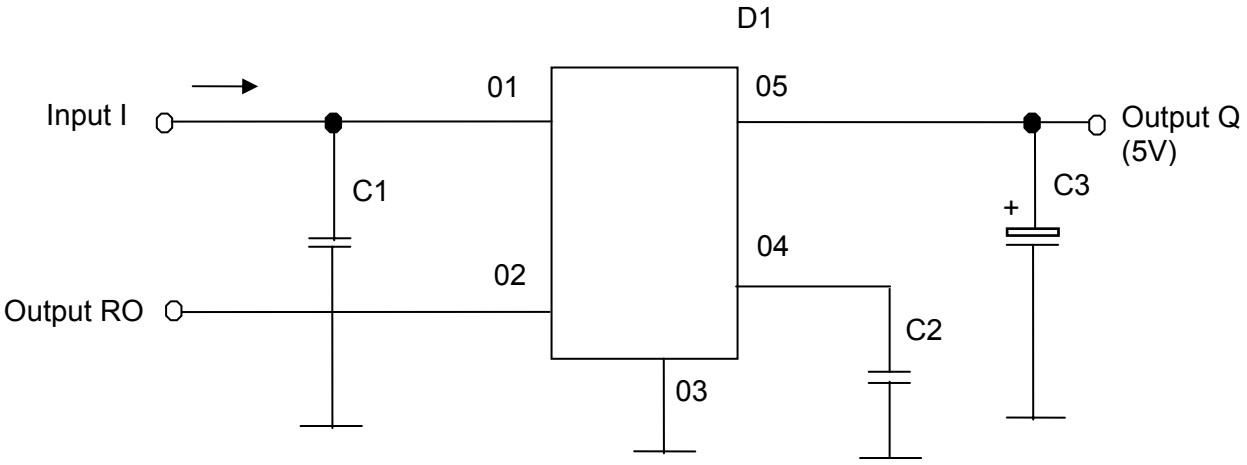


Fig. 4 – Operation time diagram of ILE4270G, ILE4270S



C1 – Capacitor 470 nF ± 20 %

C2 – Capacitor 100 nF ± 20 %

C3 – Electrolytic capacitor 22 µF ± 20 %

D1 - IC

Fig.5 – Application diagramm ILE4270G, ILE4270S

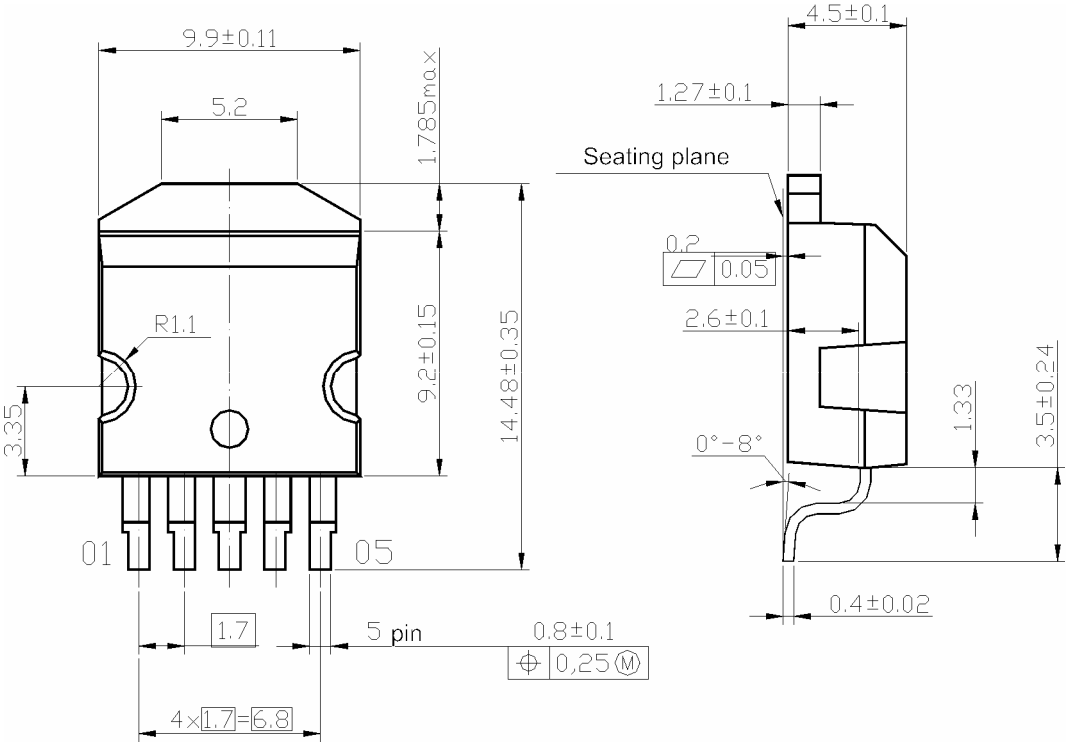


Fig 5 – P-TO263-5-1 package outline

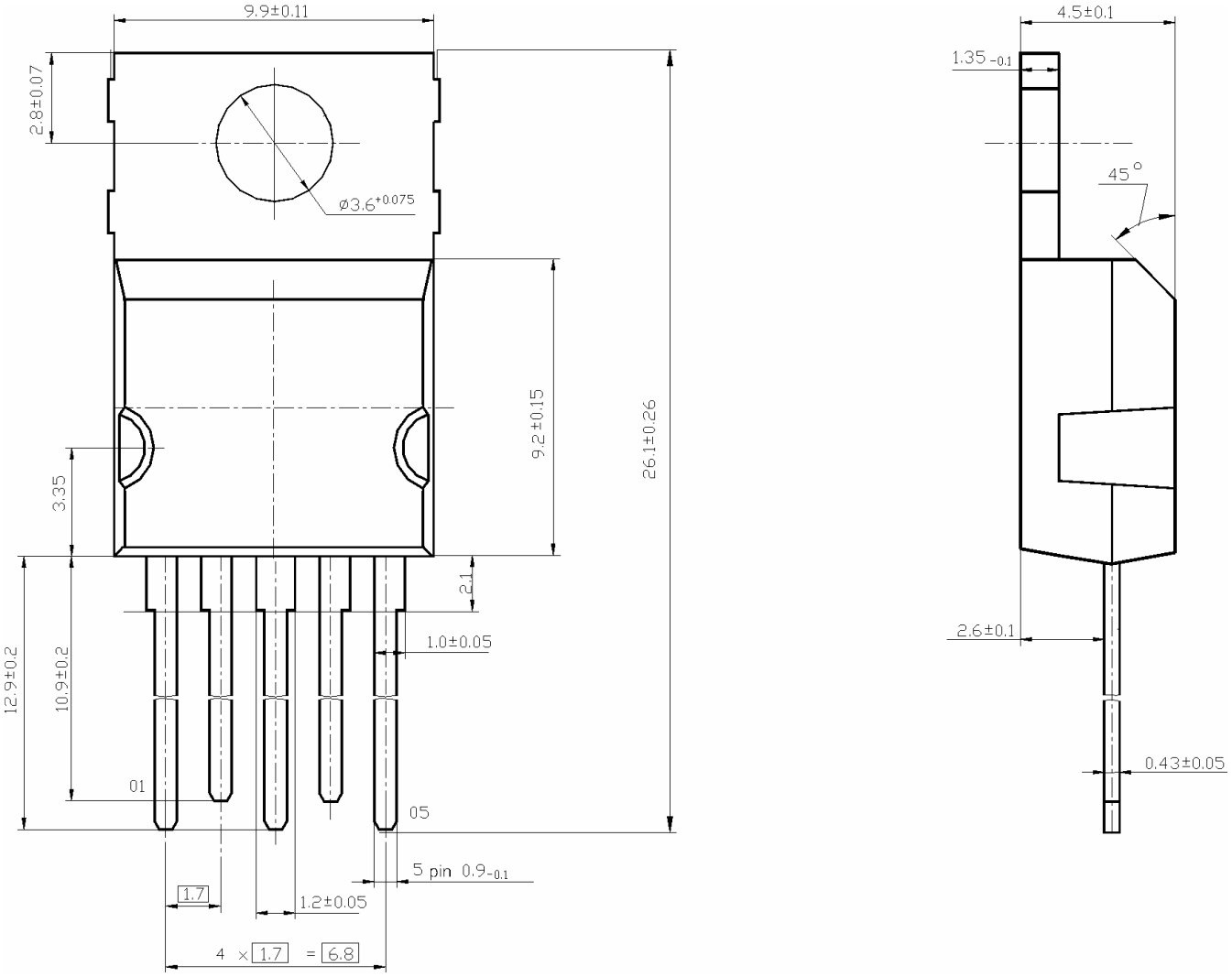
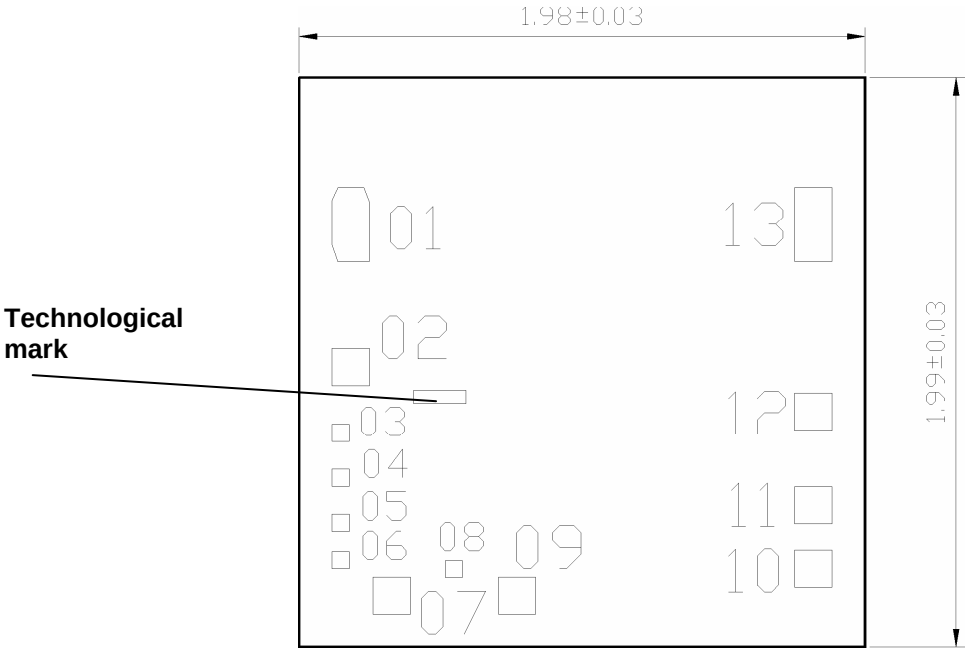


Fig. 6 – P-TO220-5-12 package outline



Technological mark on chip «4270.» has coordinates, mm: left bottom corner x = 0,290 , y = 0,817.
Chip thickness is 0,35±0,02.
Chip outline drawing

Table 6 Contact pad location table

Contact pad number	Coordinates (Left bottom corner), mm	
	X	Y
01	0,1155	1,3465
02	0,1155	0,9135
03	0,1155	0,7175
04	0,1155	0,560
05	0,1155	0,4025
06	0,1155	0,2725
07	0,2595	0,1135
08	0,512	0,2415
09	0,6975	0,1135
10	1,7345	0,2075
11	1,7345	0,4285
12	1,7345	0,7575
13	1,7345	1,3465

Notes
1. Coordinates and size of the contact pads are given by the layer «Passivation»
2 Sizes of contact pads are
pads 03-06, 08 - 0,060 x 0,060 mm,
pads 02, 07, 09 -12 - 0,130 x 0,130 mm.
pads 01, 13 - 0,130 x 0,260 mm
3 Bevel of three corners of the first contact pad is (24 ± 2) μm