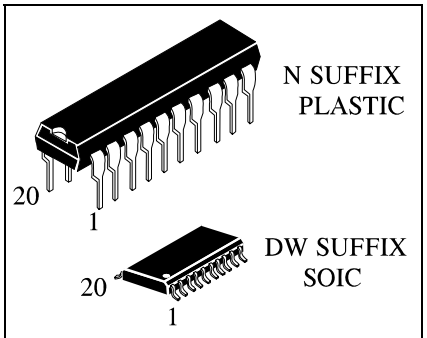
IN74ACT323

8-Bit Bidirectional Universal Shift Register with Parallel I/O

High-Speed Silicon-Gate CMOS



ORDERING INFORMATION
IN74ACT323N Plastic
IN74ACT323DW SOIC
T_A = -40° to 85° C for all packages

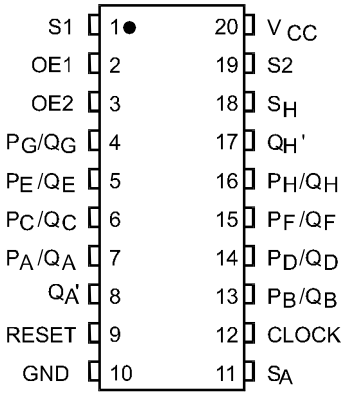
The IN74ACT323 is identical in pinout to the LS/ALS323, HC/HCT323. The IN74ACT323 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The IN74ACT323 features a multiplexed parallel input/output data port to achieve full 8-bit handling in a 20 pin package. Due to the large output drive capability and the 3-state feature, this device is ideally suited for interface with bus lines in a bus-oriented system.

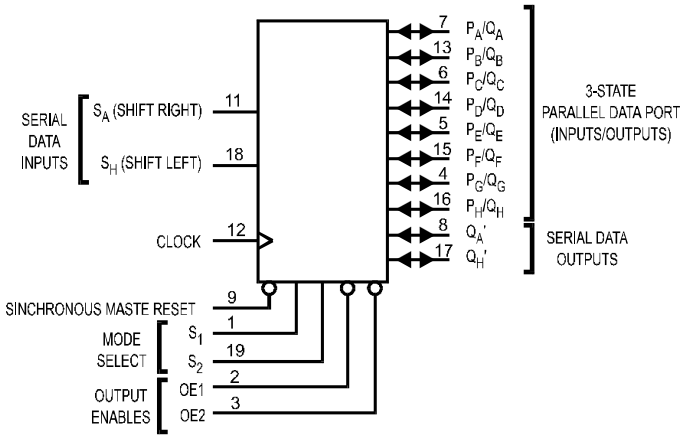
Two Mode-Select inputs and two Output Enable inputs are used to choose the mode of operation as listed in the Function Table. Synchronous parallel loading is accomplished by taking both Mode-Select lines, S_1 and S_2, high. This places the outputs in the high-impedance state, which permits data applied to the data port to be clocked into the register. Reading out of the register can be accomplished when the outputs are enabled. The active-low synchronous Reset overrides all other inputs.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA; 0.1 μA @ 25°C
- Outputs Source/Sink 24 mA

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 20 = V_{CC}
PIN 10 = GND

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Temperature, All Package Types		-40	+85	°C
I_{OH}	Output Current - High			-24	mA
I_{OL}	Output Current - Low			24	mA
t_r, t_f	Input Rise and Fall Time *	V_{CC} =4.5 V	0	10	ns/V
	(except Schmitt Inputs)	V_{CC} =5.5 V	0	8.0	

* V_{IN} from 0.8 V to 2.0 V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limits		Unit
				25 °C	-40°C to 85°C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}= 0.1 V or V_{CC}-0.1 V	4.5 5.5	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}= 0.1 V or V_{CC}-0.1 V	4.5 5.5	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$I_{OUT} \leq$ -50 μA	4.5 5.5	4.4 5.4	4.4 5.4	V
		*V_{IN}=V_{IH} or V_{IL} I_{OH}=-24 mA I_{OH}=-24 mA	4.5 5.5	3.86 4.86	3.76 4.76	
V_{OL}	Maximum Low-Level Output Voltage	$I_{OUT} \leq$ 50 μA	4.5 5.5	0.1 0.1	0.1 0.1	V
		*V_{IN}= V_{IH} or V_{IL} I_{OL}=24 mA I_{OL}=24 mA	4.5 5.5	0.36 0.36	0.44 0.44	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	5.5	±0.1	±1.0	μA
ΔI_{CCT}	Additional Max. I_{CC}/Input	V_{IN}=V_{CC} - 2.1 V	5.5		1.5	mA
I_{OZ}	Maximum Three-State Leakage Current	V_{IN} (OE)= V_{IH} or V_{IL} V_{IN} =V_{CC} or GND V_{OUT} =V_{CC} or GND	5.5	±0.6	±6.0	μA
I_{OLD}	+Minimum Dynamic Output Current	V_{OLD}=1.65 V Max	5.5		75	mA
I_{OHD}	+Minimum Dynamic Output Current	V_{OHD}=3.85 V Min	5.5		-75	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND	5.5	8.0	80	μA

* All outputs loaded; thresholds on input associated with output under test.
+Maximum test duration 2.0 ms, one output loaded at a time.

AC ELECTRICAL CHARACTERISTICS(V_{CC}=5.0 V ± 10%, C_L=50pF,Input t_r=t_f=3.0 ns)

Symbol	Parameter	Guaranteed Limits				Unit
		25 °C		-40°C to 85°C		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency (Figure 1)	120		110		MHz
t_{PLH}	Propagation Delay, Clock to Q_A' or Q_H' (Figure 1)	5.0	12.5	4.0	14.0	ns
t_{PHL}	Propagation Delay, Clock to Q_A' or Q_H' (Figure 1)	5.0	13.5	4.5	15.0	ns
t_{PLH}	Propagation Delay, Clock to Q_A thru Q_H (Figure 1)	5.0	12.5	4.5	13.5	ns
t_{PHL}	Propagation Delay, Clock to Q_A thru Q_H (Figure 1)	6.0	15.0	5.0	16.5	ns
t_{PZH}	Propagation Delay , OE1, OE2 to Q_A thru Q_H (Figure 3)	3.5	11.0	3.0	12.5	ns
t_{PZL}	Propagation Delay , OE1, OE2 to Q_A thru Q_H (Figure 3)	3.5	11.5	3.0	13.0	ns
t_{PHZ}	Propagation Delay , OE1, OE2 to Q_A thru Q_H (Figure 3)	4.0	12.5	3.0	13.5	ns
t_{PLZ}	Propagation Delay , OE1, OE2 to Q_A thru Q_H (Figure 3)	3.0	11.5	2.5	12.5	ns
C_{IN}	Maximum Input Capacitance	4.5		4.5		pF

		Typical @25°C,V_{CC}=5.0 V	
C_{PD}	Power Dissipation Capacitance	170	pF

TIMING REQUIREMENTS(V_{CC}=5.0 V ± 10%, C_L=50pF, Input t_r=t_f=3.0 ns)

Symbol	Parameter	Guaranteed Limits		Unit
		25 °C	-40°C to 85°C	
t_{su}	Minimum Setup Time, Mode Select S1 or S2 to Clock (Figure 4)	5.0	5.0	ns
t_{su}	Minimum Setup Time, Data Inputs P_A thru P_H to Clock (Figure 4)	4.0	4.5	ns
t_{su}	Minimum Setup Time, Data Inputs S_A, S_H to Clock (Figure 4)	4.5	5.0	ns
t_{su}	Minimum Setup Time, Reset to Clock (Figure 2)	2.5	2.5	ns
t_h	Minimum Hold Time, Clock to Mode Select S1 or S2 (Figure 4)	1.5	1.5	ns
t_h	Minimum Hold Time, Clock to Data Inputs P_A thru P_H (Figure 4)	1.0	1.0	ns
t_h	Minimum Hold Time, Clock to Data Inputs S_A, S_H (Figure 4)	1.0	1.0	ns
t_h	Minimum Hold Time, Clock to Reset (Figure 2)	1.0	1.0	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	4.0	4.5	ns

FUNCTION TABLE

Inputs									Response									
Mode	Reset	Mode Select		Output Enables		Clock	Serial Inputs		P_A/Q_A	P_B/Q_B	P_C/Q_C	P_D/Q_D	P_E/Q_E	P_F/Q_F	P_G/Q_G	P_H/Q_H	Q_A'	Q_H'
		S_2	S_1	OE1↑	OE2↑		D_A	D_H										
Reset	L	X	L	L	L	⎍	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	⎍	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	Q_A through Q_H=Z								L	L
Shift Right	H	L	H	H	X	⎍	D	X	Shift Right: Q_A through Q_H=Z; $D_A \rightarrow F_A$; $F_A \rightarrow F_B$; etc								D	Q_G
	H	L	H	X	H	⎍	D	X	Shift Right: Q_A through Q_H=Z; $D_A \rightarrow F_A$; $F_A \rightarrow F_B$; etc								D	Q_G
	H	L	H	L	L	⎍	D	X	Shift Right: $D_A \rightarrow F_A = Q_A$; $F_A \rightarrow F_B = Q_B$; etc								D	Q_G
Shift Left	H	H	L	H	X	⎍	X	D	Shift Left: Q_A through Q_H=Z; $D_H \rightarrow F_H$; $F_H \rightarrow F_G$; etc								Q_B	D
	H	H	L	X	H	⎍	X	D	Shift Left: Q_A through Q_H=Z; $D_H \rightarrow F_H$; $F_H \rightarrow F_G$; etc								Q_B	D
	H	H	L	L	L	⎍	X	D	Shift Left: $D_H \rightarrow F_H = Q_H$; $F_H \rightarrow F_G = Q_G$; etc								Q_B	D
Parallel Load	H	H	H	X	X	⎍	X	X	Parallel Load: $P_N \rightarrow F_N$								P_A	P_H
Hold	H	L	L	H	X	X	X	X	Hold: Q_A through Q_H=Z; F_N=F_N								P_A	P_H
	H	L	L	X	H	X	X	X	Hold: Q_A through Q_H=Z; F_N=F_N								P_A	P_H
	H	L	L	L	L	X	X	X	Hold: $Q_N = Q_H$								P_A	P_H

Z = high impedance

D = data on serial input

F = flip-flop (see Logic Diagram)

↑ When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

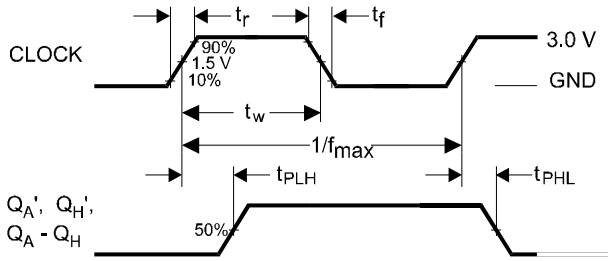


Figure 1. Switching Waveform

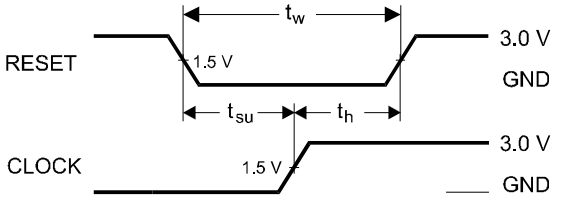


Figure 2. Switching Waveform

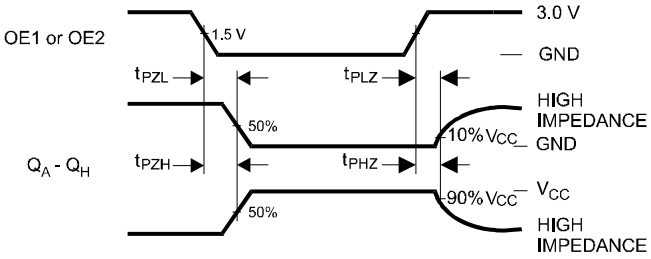


Figure 3. Switching Waveform

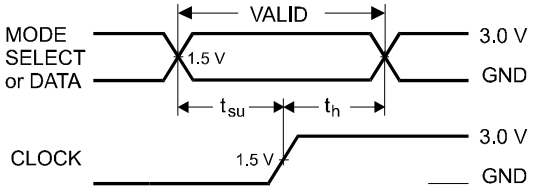


Figure 4. Switching Waveform

EXPANDED LOGIC DIAGRAM